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"STUDY OF HOT-ELECTRON EFFECTS, BREAKDOWN AND RELIABILITY IN FETS, HEMTS, AND HBT'S"

Final Technical Report

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August 1998

United States Army

EUROPEAN RESEARCH OFFICE OF THE U.S. ARMY

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Summary

The objective of this project has been the understanding of the physical limitation of GaAs, InP and wide-bandgap semiconductors through experimental and the theoretical evaluation. In particular evaluation of scaling properties, hot electron effects, breakdown phenomena and failure mechanisms in AlGaAs/InGaAs and InAlAs/InGaAs High Electron Mobility Transistors (HEMT's) and in InAlAs/InGaAs Heterojunction Bipolar Transistors (HBT's) has been carried out. Physical phenomena studied in this work include: (i) impact ionization; (ii) short-channel effects; (iii) quantum confinement and real space transfer; (iv) failure mechanisms of GaAs- and InP-based devices. Devices adopting wide bandgap semiconductors (SiC) have also been studied.

We have studied the impact ionization coefficient in $In_{0.53}Ga_{0.47}As$ material by using a suitable HBT structure. A positive temperature coefficient has been found in this material. Theoretical work has included the development of ionization models for InGaAs layers, and the inclusion of non local ionization effects into drift-diffusion simulators.

Hot-electron effects in pseudomorphic AlGaAs/InGaAs HEMTs has also been studied. The behaviour of electroluminescence at high fields has been analyzed and the presence of a band-to-band recombination peak has been demonstrated. On the theoretical side, we have used the self consistent HEMT Monte Carlo code to study short channel effects, impact ionization and electroluminescence in pseudomorphic HEMTs GaAs/InGaAs/AlGaAs. The analysis also demonstrate that holes generated by impact-ionization are able to reach the source and recombine there.

Accelerated tests at high V_{DS} have been carried out both in GaAs- and InP based HEMT's. Permanent degradation resulting in the development of a remarkable "kink" in the output characteristics has been found. DC, pulsed, low-frequency AC and DLTS measurements demonstrate that the failure mechanism consists in the creation of deep levels. We will also report on the elimination of the kink effect and hot-electron degradation in InP-based HEMT's which results from the insertion of an InP etch stop layer on top of the InAlAs donor layer.

Hot electron behaviour of silicon carbide JFET has been analyzed in detail. The JFET gate current I_G, due to collection of holes generated by impact-ionization has been measured. The multiplication factor $| I_G | / I_D$ has been found to decrease with temperature in agreement with the usual decrease of the impact ionization coefficient at increasing the temperature. The breakdown voltage, however decreases at increasing the temperature, and an anomalous kink effect occurs at low temperature. Both anomalies seems to be related with an incomplete ionization of donor and acceptor impurities and with the presence of deep levels.

List of Keywords
Microwave devices;
High Electron Mobility Transistors (HEMT's);
Heterojunction Bipolar Transistors (HBT's);
Silicon Carbide Junction Field Effect Transistors (SiC JFET's);
Gallium Arsenide;
Indium Phosphide;
Impact Ionization;
Breakdown Voltage;
Reliability.

Contents

Introduction

Both civil and military applications of microwave and millimeter wave systems require the development of basic devices having extremely high transient frequencies, low-noise performances or good power handling capabilities and excellent reliability. In the last few years, the continuous improvement of the microwave performance capabilities of GaAs MESFET's and of a variety of HEMT devices and circuits has enabled the development of advanced military systems which, in turn, has favoured the assessment of manufacturing capabilities to serve both the military and commercial marketplaces [1, 2, 3]. A large effort has been also devoted by defense industries and by the U.S. Department of Defense to the improvement of HBT technology, culminating in the development of several digital and analog applications [4, 5, 6, 7].

In the last years, new technologies have demonstrated improved performances and reliability; in particular, the low-noise and power performances of pseudomorphic AlGaAs/InGaAs HEMTs have been improved, allowing applications in systems up to 60 GHz. Double recess structures with fairly high breakdown voltages (10-20 V) have been demonstrated, with power added efficiencies between 10% (around 1 W) and 50% (around 20 mW) at 60 GHz.

For higher frequencies, InP-based devices with sophisticated technological solutions are in continuous development. InP-based HEMTs, usually adopting an $In_{0.53}Ga_{0.47}As$ channel have better noise figures than GaAs-based HEMT's for all frequencies, and better power added efficiencies at 94 GHz and beyond; for sub-100 mW demonstrations, InP features PAE values in the 20 to 35% range. In contrast, GaAs does not exceed 15% [8]. Due to the narrow bandgap of $In_{0.53}Ga_{0.47}As$, InP-based HEMTs are plagued by low breakdown voltages. In particular, a high on-state breakdown is crucial to enhance power output in InP-based HEMTs [9]; several technological improvements have been suggested to control and reduce impact-ionization, including InGaAs/InP composite channels [10, 11], asymmetric recess [12], double recess [13], and p-body contacts in order to remove excess holes [14]. A further complication comes from the thermal coefficient of impact-ionization of $In_{0.53}Ga_{0.47}As$, which increases at increasing the temperature [11, 15], thus possibly inducing a positive electro-thermal feedback leading to device breakdown and burn-out.

Narrow bandgap semiconductors clearly dominate applications at extremely high frequencies. On the opposite hand, for very high power applications at fairly low frequencies (i.e. for radar applications at C, S and X bands and for base station transmitters at L and S bands), wide band-gap materials such as GaN and SiC have emerged as leading candidates. [16, 17, 18, 19, 20, 21, 22, 23].

Silicon carbide devices (MESFETs and SITs, Static Induction Transistors) can produce RF power densities in excess of what is possible with GaAs MESFETs or HEMTs. A 53 W CW S-band (3 GHz) 4H-SiC MESFET having a PAE = 37% has been recently demonstrated [24]; 6H-SiC MESFETs that can operate at frequencies up to X band (10 GHz) have been produced with 2.5 W/mm and power added efficiency on the order of 45% at 6 GHz [25].

The breakdown mechanisms of SiC devices are different from those of narrow band-gap semiconductors, possibly involving the contribution of non-completely ionized impurities [21]. Further studies concerning impact-ionization and related effects in wide band-gap semiconductors are needed.

The purpose of this work was the theoretical and experimental study of the main factors which can limit the rf power handling capabilities of GaAs-based and InP-based HEMTs. A preliminary study of the breakdown characteristics of 6H-SiC JFETs and of their dependence on temperature was also

carried out.
In particular, we addressed the physical phenomena which can affect the maximum operating voltage of the above mentioned devices, i.e.:

- impact-ionization
- tunneling effects
- short-channel effects
- quantum confinement and real-space-transfer
- electro-thermal effects
- interaction between holes generated by impact-ionization and trapping effects

Since degradation mechanisms can also be accelerated by operating the devices at high voltages, an extensive study of the effects of the reliability of pseudomorphic and InP-based HEMTs submitted to aging tests at high V_{DS} has also been carried out.

Results can be summarized as follows:

- In order to obtain a correct model of multiplication effects in HEMT devices, the impact-ionization coefficient of $In_{0.53}Ga_{0.47}As$ and its dependence on temperature have been measured by means of suitable InAlAs/InGaAs Heterojunction Bipolar Transistors; a "delay" analytical model has been developed to take into account the dead space effect and correct impact-ionization data.
- A complete experimental characterization of hot-carrier effects in pseudomorphic HEMTs has been carried out. These data demonstrate the effect of the accumulation of generated holes at the source end of the devices in determining kink effects and premature breakdown.
- A self-consistent many-particle ensemble Monte Carlo (MC) simulator was used to evaluate theoretically hot carrier effects. A three-valley nonparabolic band structure has been used for each material layer. The MC procedure is coupled with a two-dimensional Poisson solver and includes impact-ionization of both electrons and holes in the InGaAs and in the AlGaAs layers. Monte Carlo simulations have been used here for the first time to evaluate dynamic impact-ionization effects and to study the influence of device design on breakdown phenomena.
- The electroluminescence spectra of HEMT have been experimentally evaluated and have been calculated within a tight-binding (TB) approach.
- The reliability of PM-HEMT and InP-based HEMTs submitted to hot carrier DC testing at high V_{DS} has been extensively studied, identifying specific failure mechanisms related to the generation of deep levels in the gate recess region or at the surface of the gate-drain access region.
- Impact-ionization and breakdown effects have been studied in 6H SiC JFETs grown on Lely substrates. The data presented here demonstrate that incompletely-ionized impurities can generate anomalous effects such as frequency dispersion of the transconductance, kink effects, and anomalous behaviour of the thermal coefficient of the breakdown voltage.

Specific results are summarized in the Conclusions.

The report is organized as follows. The first Section describes the experimental analysis and Monte Carlo modeling of hot carrier effects in GaAs-based pseudomorphic HEMTs and InP-based HEMTs. A second Section is devoted to the results concerning the reliability analysis of PM-HEMTs and InP-based HEMT's. Finally, we present the results related with impact-ionization and incomplete ionization of impurities in 6H SiC JFETs. Conclusions follow.

List of Publications

G. Meneghesso, T. Grave , M. Manfredi, M. Pavesi, C. Canali and E. Zanoni,
"Electroluminescence analysis of multiplication effects in pseudomorphic HEMT's",
22th European Workshop on Compound Semiconductor Devices and Integrated Circuits WOCSDICE 1998, pp. 24-25, Zeuthen, Germany, May 24-27, 1998.

G. Meneghesso, A. di Carlo, M. Manfredi, M. Pavesi, C. Canali and E. Zanoni,
"Characterization of hole transport phenomena in AlGaAs/InGaAs HEMT's biased in impact-ionization regime",
56th Annual Device Research Conference, pp. 36-37, University of Virginia, Charlottesville, VA, June 1998.

G. Meneghesso, A. Bartolini, G. Verzellesi, A. Cavallini, A. Castaldini, C. Canali, E. Zanoni,
"Breakdown and low-temperature anomalous effects in 6H SiC JFETs",
Tecnical Digest of IEEE International Electron Devices Meeting 1998, IEDM98, pp. 695-698, S. Francisco, CA, December 6-9, 1998.

G. Meneghesso, A. Neviani, R. Oesterholt, M. Matloubian, T. Liu, J. Brown, C. Canali and E. Zanoni,
"On-State and Off-State Breakdown in InGaAs/InP Composite-Channel HEMTs with Variable InGaAs Channel Thickness",
IEEE Trans. on Electron Devices, Vol. 46, No. 1, pp. 2-9, 1999.

G. Meneghesso, A. Cavallini, A. Castaldini, G. Verzellesi, C. Canali and E. Zanoni,
"High field and low temperature behaviour of Lely-grown 6H SiC buried gate JFETs",
Submitted to WSSM1, 1st International Workshop on Semiconducting and Superconducting Materials Turin, February 17-19, 1999.

G. Meneghesso, T. Grave, M. Manfredi, M. Pavesi, C. Canali, E. Zanoni,
"Analysis of hot carrier transport in AlGaAs/InGaAs pseudomorphic HEMT's by means of electroluminescence",
Submitted to IEEE Trans. on Electron Devices.

Part I

Measurement and Modeling of the impact-ionization coefficient of GaAs and of InGaAs Lattice Matched on InP and of its temperature coefficient

Chapter 1

Measurements and modeling of the impact ionization coefficient of $In_{0.53}Ga_{0.47}As$

1.1 Impact Ionization on $In_{0.53}Ga_{0.47}As$ HBTs

1.1.1 Introduction

The study of the ionization phenomena in InGaAs is of great importance both from the practical and theoretical point of view. In fact, the current-voltage operating range and the noise figure of InGaAs-based devices are adversely affected by the onset of impact ionization [26], which is enhanced due to the low energy gap of this material. Theoretical [27] and experimental [28, 29] studies have predicted and demonstrated a weak field dependence of the electron ionization coefficient α_n in $In_{0.53}Ga_{0.47}As$ at medium-low electric fields (below 200 KV/cm). Furthermore, as opposed to the behavior observed in most semiconductors, a reduction of the common-emitter breakdown voltage BV_{CE0} with increasing temperature has been observed [28, 30] in InGaAs/InP HBT's. An increase of ionization current with temperature has also been reported in $In_{0.53}Ga_{0.47}As$-channel HEMT's [31]. The understanding of this behavior is of great importance due to the possible onset of a positive feedback loop between power dissipation and ionization-induced increase of output current. This may also be an important issue in electro-thermal modelling of $In_{0.53}Ga_{0.47}As$-based devices.

In this work, we report data on both weak field dependence of the electron ionization coefficient α_n at medium-low electric fields (below 200 KV/cm) and on the positive temperature dependence of α_n in $In_{0.53}Ga_{0.47}As$, measured in $In_{0.53}Ga_{0.47}As$/InP HBT's.

1.1.2 Samples and Measurement Technique

The devices used in this work were npn $In_{0.53}Ga_{0.47}As$-collector HBT's fabricated at Hughes Research Laboratories. The devices are grown on a semi-insulating InP substrate, with an n^+ $In_{0.53}Ga_{0.47}As$ sub-collector, a 300 nm-thick $In_{0.53}Ga_{0.47}As$ collector with 5×10^{15} cm^{-3} n-doping, a 50 nm-thick $In_{0.53}Ga_{0.47}As$ base with 3×10^{19} cm^{-3} p^+-doping, an InAlAs/InGaAs superlattice grading, and a 120 nm-thick n-doped InAlAs emitter. The emitter and collector junction area are 2×10 μm^2 and 5×14 μm^2, respectively.

The common-emitter breakdown voltage BV_{CE0} in $In_{0.53}Ga_{0.47}As$-collector HBT's has been demonstrated to decrease with increasing temperature [28, 30]. We demonstrate here that this anomalous temperature behavior is due to a positive dependence of the electron impact ionization coefficient α_n on temperature in $In_{0.53}Ga_{0.47}As$.

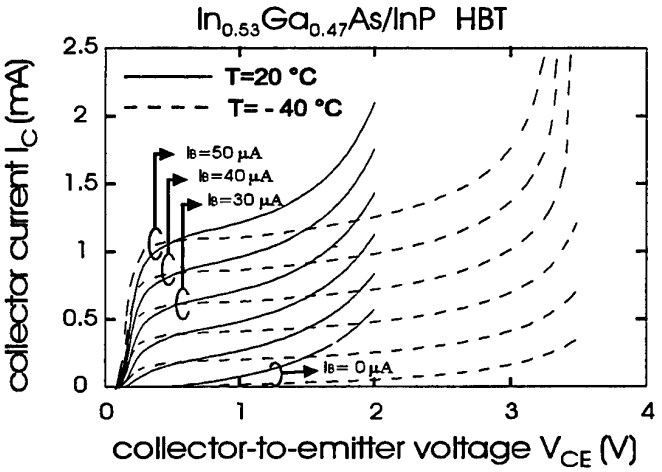

Figure 1.1: Collector current, I_C vs. the collector to emitter voltage V_{CE} at different temperatures in a studied $In_{0.53}Ga_{0.47}As$ HBT.

The experimental technique is based on the measurement of the base current change ΔI_B with V_{CB} and the collector multiplication factor M–1 in HBT's biased in common base configuration, as described in [29, 32]. α_n is then calculated as the ratio between M–1 and the collector thickness W_C, under the following assumptions: (i) $\alpha_n \geq \alpha_p$, where α_p is the hole ionization coefficient; (ii) M–1 $\ll 1$; (iii) the electric field is constant in the collector depletion region; (iv) α_n is a function of the local electric field. The validity of these assumptions is thoroughly discussed in [29, 32] and will not be repeated here. We only point out that this technique allows an unprecedented sensitivity in the extraction of α_n at low electric fields.

Each measurement was performed at a fixed temperature varying V_{CB} from 0 to 5 V. Measurements were repeated at different temperatures in the range $-100°C \div +50°C$. Great care has been taken in order to estimate and minimize the contributions to the measurement coming from phenomena other than impact ionization. In particular, the effect of base width modulation (Early effect) is negligible [29]; base-collector reverse current I_{CB0} is well below 5% of ΔI_B at all temperatures; the effect of device self-heating due to power dissipation was ruled out by repeating the measurement at different values of I_E (from 10 to 100 μA) and observing that the values of M–1 did not change; the common-base current gain α_F shows a negative dependence on temperature.

1.1.3 Results and Discussion

The negative temperature dependence of BV_{CE0}, reported in [28, 30], is also observed in our devices as shown in Fig. 1.1. Unfortunately, common-emitter breakdown behavior could not be clearly attributed to the effect of impact ionization alone in our case. In fact, despite the devices demonstrate excellent stability and low base-collector reverse current when operated outside the breakdown region, a permanent increase of I_{CB0}, not compatible with M–1 measurement, was observed whenever a device was biased close to breakdown voltage in common emitter configuration. This increase of I_{CB0} was attributed to accelerated degradation of the base-collector diode.

We verified carefully that no degradation took place during the common-base measurements of ΔI_B, and that I_{CB0} remained within 5% of ΔI_B, as stated in the previous section. This is not surprising, since ΔI_B measurements were carried out up to $V_{CB} = 5$ V, which is below the breakdown region were BC diode degradation takes place. Since thermally-generated leakage current I_{CB0} could also affect our measurements, the relative weight of the impact ionization component and of the leakage component of ΔI_B was evaluated by plotting ΔI_B vs I_E at fixed values of V_{CB}. The linear dependence

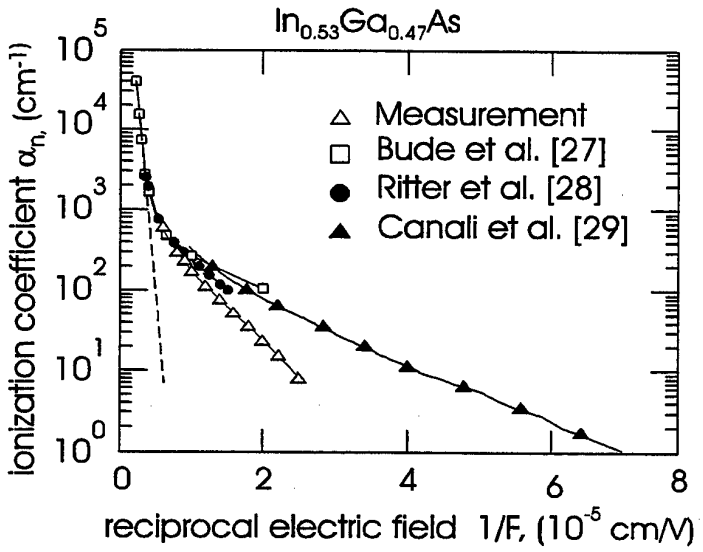

Figure 1.2: Impact ionization coefficient evaluated in our devices and compared with the values reported in literature.

of ΔI_B on I_E rules out tunneling and thermal generation as multiplication mechanisms, suggesting a generation mechanism activated by the primary electron current $\alpha_F I_E$ entering the collector region, such as impact ionization. Furthermore, starting from the standard collector multiplication model [33], it is straightforward to show that:

$$\Delta I_B(V_{CB}) = I_B(V_{CB} = 0) - I_B(V_{CB}) = M \cdot I_{CB0} + (M-1) \cdot \alpha_F \cdot I_E \tag{1.1}$$

and thus the y-axis intercept of the ΔI_B vs I_E curve yields the value of $M \cdot I_{CB0}$, which is an upper bound to the value of $I_{CB0}(V_{CB})$, since $M \geq 1$. This allowed us to verify that I_{CB0} is below 5% of ΔI_B(measured at $I_E = 100\ \mu A$) at all temperatures.

Then it makes sense to define a multiplication factor M–1 as the ratio of the multiplication current ΔI_B and the primary current $I_C - |\Delta I_B|$ [29, 32]. Measurement of M–1 in present devices demonstrates that M–1 monotonically increases with V_{CB} and with temperature. Possible spurious contributions to ΔI_B which may give a positive dependence on temperature have been discussed in the previous section and ruled out for the present measurement.

The final result of the measurement procedure is a matrix of α_n values taken at different temperatures and average collector electric field. At room temperature, the measured behavior of α_n against the reciprocal of the average electric field is in good agreement with that obtained by Ritter et al., [28], and by Canali et al., [29], as shown in Fig. 1.2. In particular, the medium-low-field tail (i. e. below 200 kV/cm) of the α_n curve is characterized by a weak dependence on the electric field, as predicted by Bude and Hess [27]. They explain this anomalous behaviour in terms of the density of states in the conduction band of $In_{0.53}Ga_{0.47}As$. $In_{0.53}Ga_{0.47}As$ in fact is characterized by a low energy gap (0.75 eV) and a high separation between the L valley minimum and the Γ valley minimum ($\sim$ 0.55 eV). An electron with energy just about the ionization energy threshold will have its final state in the Γ valley after an ionization event. The same is true for the ionized electrons. Since the density of the state in the Γ valley minimum is low, only a small number of final state combination will satisfy the energy and pseudomomentum conservation at the same time. Consequently, the ionization rate is limited by the number of possible final states, and shows a weak dependence on the electric field until the energy of the ionizing electrons is sufficiently high that it allows the states in the L valley to become the

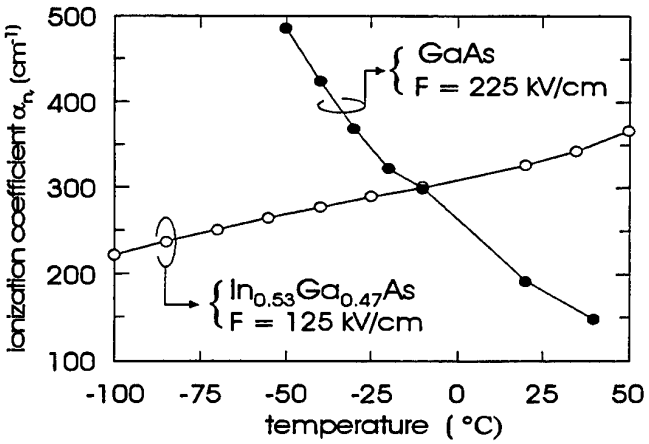

Figure 1.3: Electron ionization coefficient α_n vs temperature measured in $In_{0.53}Ga_{0.47}As$ at a fixed electric field F = 125 KV/cm (open circles) and in GaAs at F = 225 KV/cm (filled circles).

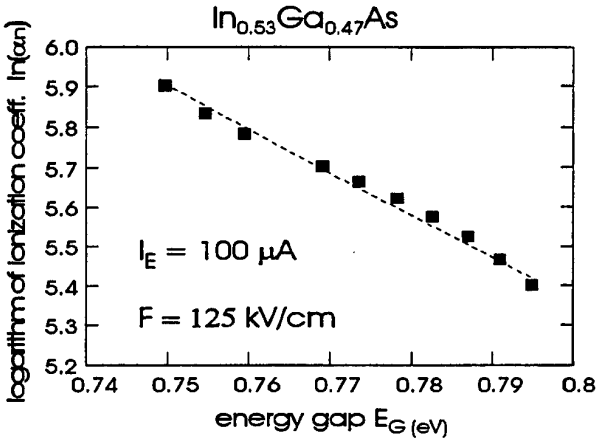

Figure 1.4: Electron ionization coefficient α_n vs energy gap E_G in $In_{0.53}Ga_{0.47}As$ at a fixed electric field F = 125 KV/cm.

final state. From this point, the number of possible final states increases dramatically, resulting in a stronger dependence of the ionization rate on the electric field.

The key result of this work is the positive temperature dependence of α_n, shown in Fig. 1.3 (open circles) at an average electric field F=125 KV/cm, which is opposite with respect to that observed in most other semiconductors. As an example, in the same figure we also reported the corresponding behavior of α_n that we measured in GaAs at a different field F=225 KV/cm (filled squares) using the HBT's described in [32]. The "ordinary" behavior observed in GaAs, that is, the decrease of α_n with temperature, is attributed to temperature-enhanced phonon scattering reducing the population of the primary electrons high energy tail. Indeed, popular models of impact ionization like Okuto-Crowell's [34] can easily fit both electric field and temperature behavior of α_n in GaAs. On the contrary, fitting the medium-low electric field tail (below 200 KV/cm) of α_n in $In_{0.53}Ga_{0.47}As$ with the same model yields unrealistic values of mean free path and ionization threshold energy, and a negative temperature coefficient of α_n.

The failure of this model may be linked to the fact that, according to Bude and Hess [27], at low electric fields impact ionization in $In_{0.53}Ga_{0.47}As$ is limited by the low density of states near the Γ-valley minimum and not by the number of primary electrons with energy above the ionization threshold. In this picture, temperature-increased phonon scattering, which reduces the population of

the high energy tail of the electron distribution, would have little effect on the ionization rate. On the contrary, the reduction of the energy gap E_G (and thus of the ionization threshold energy) with increasing temperature seems to play a dominant role on α_n temperature behavior. This is clear from Fig. 1.4, in which the natural logarithm of α_n is plotted against E_G, showing a negative exponential relation.

It should be stressed that these anomalous behaviours of the impact ionization coefficient (at low electric field and as a function of temperature) must be deeply understood in order to fully characterize the breakdown behaviour of $In_{0.53}Ga_{0.47}As$-based devices.

1.2 Modeling the impact ionization of $In_{0.53}Ga_{0.47}As$. The delay model

Device simulation has become a fundamental part in the development and optimization of electronic devices. Next to standard approaches such as the Drift Diffusion (DD) method [35], which has lead to several commercial software packages, newer techniques are also available, ranging from hydrodynamical approaches to particle-based simulations, such as the Monte Carlo (MC) or the Cellular Automaton (CA) methods [36, 37, 38]. In general one pays the enhanced physical content of the latter approaches with a heavier computational load. Thus is particularly true in the presence of high electric fields. While physical simulators require then an accurate description of high energy effects, DD methods can rely on simplified phenomenological approaches. As above mentioned, however, conventional models fail to describe the impact ionization coefficient of $In_{0.53}Ga_{0.47}As$. In this section we describe a model for impact-ionization which allow us to exploit the speed advantages of DD methods while incorporating the main physical features of the impact-ionization process.

1.2.1 Impact Ionization in Drift Diffusion and Monte Carlo Simulators

Impact-ionization is the phenomenon by which a hot carrier colliding with a valence electron creates a new pair of carriers, both available for conduction. An accurate model of impact-ionization must account for the high energy behaviour of carriers, since the threshold for the process is at least equal to the energy gap of the semiconductor under consideration. The best treatment in terms of physical accuracy is provided by the MC method, which typically includes impact-ionization by associating to each carrier ionization probability per unit time, dependent on the carrier status (energy, velocity, momentum etc.). Several levels of refinement are possible, based on simplified bands and phenomenological impact-ionization rates , or on complete bands and microscopical impact-ionization rates. The latter approach has been applied mainly to bulk semiconductors, due to its numerical complexity, while the former one can be applied to devices. Recently, a MC analysis has been presented for an AlGaAs/GaAs Heterojunction Bipolar Transistor (HBT) [39, 40], which perfectly reproduced available experimental results both on the multiplication factor as well as on the electroluminescence spectra of the device in a near breakdown regime [32, 41, 42]. There, a three valley non-parabolic model was implemented for electrons and holes, together with the Kane model for impact-ionization. The main conclusions of that work have been:

1. The average energy and the ionization coefficients reach their maximum not at the base-collector junction, where the electric field reaches its maximum, but rather inside the collector. Such effect

is referred to as "dead space" effect [43, 44].

2. Electrons and holes gain considerable energy in the collector due to the presence of very high electric fields. As a result, the electron and hole distribution functions are very hot, leading to strong ionization processes and to radiative transitions within the conduction and the valence band, respectively [32], responsible for the observed electroluminescence.

Although the MC simulation is physically very accurate, it is also extremely time consuming. It would therefore be preferable, in the context of device modeling (and especially in the presence of ionization phenomena), to use faster numerical tools such as those based on the DD algorithm. There, the following equations are used:

$$\frac{d}{dx}\left(\epsilon\frac{dV}{dx}\right) = -\rho \tag{1.2}$$

$$J_p = qp\mu_p F - qD_p\frac{dp}{dx}\ ;\ J_n = qn\mu_n F + qD_n\frac{dn}{dx} \tag{1.3}$$

$$\frac{dJ_p}{dx} = q(G-R) = -\frac{dJ_n}{dx} \tag{1.4}$$

In Eq. 1.4, impact-ionization is accounted for by means of the generation term, G. Unfortunately such approaches do not correctly describe hot carrier and non local effects, unless ad hoc phenomenological corrections are implemented. Now we will briefly revise the widely accepted way to deal with impact-ionization in conjunction with Eqs. 1.2 ÷ 1.4.

1.2.2 Failure of 'local' models

The most common method to deal with impact-ionization phenomena in DD simulations is represented by the Local Model (LM) [45, 46]. Within such model the probability to generate a impact-ionization event in $(x, x+dx)$ for a carrier moving in the $+x$ direction is considered to be only dependent on the local electric field. Under this hypothesis, impact-ionization can be fully characterized by means of the mean free path between ionizing collisions, both for electrons, $\langle l_n \rangle$, and for holes, $\langle l_p \rangle$. The impact-ionization generation rate is linked to the $\langle l_i \rangle$ parameters and to the currents by the equations

$$qG = \alpha_L J_n + \beta_L J_p = \frac{dJ_p}{dx} = -\frac{dJ_n}{dx} \tag{1.5}$$

$$\alpha_L = \frac{1}{\langle l_n \rangle}\ ;\ \beta_L = \frac{1}{\langle l_p \rangle} \tag{1.6}$$

Here α_L and β_L represent the ionization coefficients of the LM for electrons and holes respectively. Equation (4) is usually introduced referring to a constant electric field, but can be extended to a generic field shape by assuming the impact-ionization coefficients to be function of the local electric field. Within the LM, the impact-ionization process in a given semiconductor under a specified electric field is fully characterized by a pair of real numbers, namely the ionization coefficients. Equations 1.5-1.6 can be used to link the impact-ionization coefficients (i.e. the inverse of the carriers mean free path between ionizing collision) to macroscopically observable quantities, such as the multiplication factor or the breakdown length [45]-[47]. Such equations can, in turn, be applied to extract the II coefficients as a function of the electric field from experimental data [45, 48, 49, 29, 28]

1.2.3 Monte Carlo analysis: the dead space concept

The dispersion in the experimental determinations of the impact-ionization coefficients arises from the inadequacy of the LM. In order to clarify this point we refer again to a Monte Carlo simulated experiment, by considering an electron current entering a region where a strong electric field ($F = 5{\cdot}10^7$

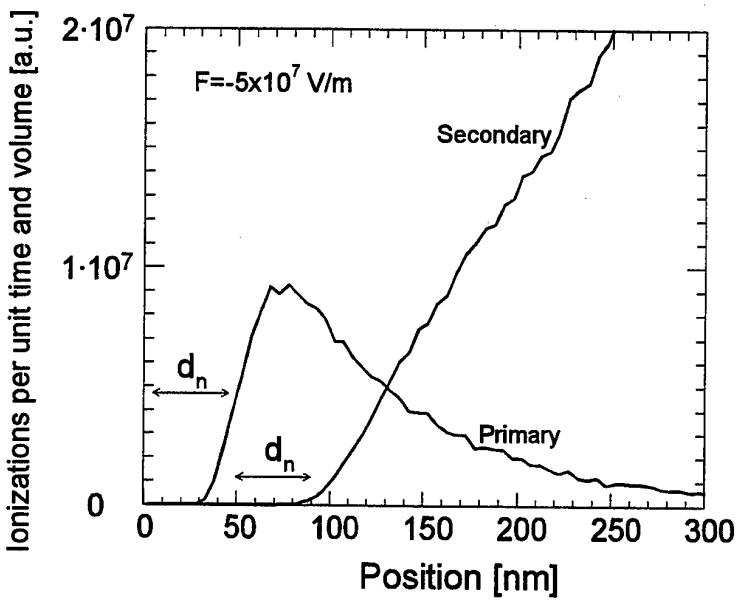

Figure 1.5: Number of ionizing collisions for unit time predicted with Monte Carlo simulation both for primary and secondary carriers. The quasi-exponential decay of the number of ionizing collisions due to the primary allows to define dead spaces and DM ionization coefficients.

V/m) is applied. For simplicity, only electron ionizations are allowed in the simulation. In Fig. 1.5, the number of ionizing collisions (per unit time and volume) is plotted as a function of position. Two types of processes are considered: the first (primary) collision of the carriers that enter in the field region, and all other (secondary) collisions, that is the further collisions of the primary carriers and those due to the carriers that are generated within the field region. Figure 1.5 clearly illustrates a fundamental physical feature of impact-ionization process, that is the "dead- space" effect: a carrier must travel a certain distance before reaching the threshold energy for impact-ionization. The "cold" injected primary electrons are not immediately available for impact-ionization. Thus, a dead-space zone (d_n) where no ionizing collisions occur is present near the contact. Equivalently, the dead-space effect can be described by the associated energy ($E_{th,n}$) gained from the carriers over the d_n length. For a constant electric field, threshold energy and dead- space are related by the equations

$$E_{th,p} = q|F|d_p \; ; \; E_{th,n} = q|F|d_n \tag{1.7}$$

for holes and electrons respectively. It is often more convenient to speak of threshold energy because such quantity is generally less sensitive to the field value than d_i, and often, as a first approximation, it is considered to be constant for a given semiconductor. $E_{th,i}$ represents the energy that a carrier must receive from the field to appreciably initiate impact-ionization. Secondary carriers came into existence only after the primary ones collide, that is not before $x = d_n$. As it can be seen on the figure, they also cannot ionize before another dead-space, that is around $x = 2d_n$. The reason of such behaviour can be understood in the light of the microscopy of the ionizing event. When the primary carrier impinges on the valence electron, it release its energy almost completely to generate a hole-electron pair roughly in rest condition. Accordingly, all secondary carriers can be assumed to restart their motion close to zero kinetic energy. This behaviour, totally neglected in the LM, must be taken into account to adequately reproduce the impact-ionization process. The mean free path between ionizing collision is only a first order description of the process. The dead space concept gives further information and, if considered in a suitable form, can add in accuracy to an adopted model, as we will see shortly.

1.2.4 Delay Model: description and implementation

We will refer here to a region with a step-constant, positive electric field. The generalization to arbitrary field profiles will be discussed later. We further assume, for the sake of simplicity, that carriers are approximately in the same rest condition after suffering an ionizing collision, or after being generated by an ionizing collision. Under these hypothesis a very general procedure for impact-ionization modeling can start by considering the spatial probability density of the ionization event, $P_n(x)$ ($P_p(x)$), for a rest electron (hole) entering the field region at $x = 0$ [50]. Clearly, $P_n(x) = 0$, $x > 0$ and $P_p(x) = 0, x < 0$. Field edge inclusion is easily accomplished with the further assumption to consider equal to 0 the impact-ionization probability soon after the field falls to 0. Under the previous assumption eqs. 1.5 must be substituted with the more general

$$\langle l_n \rangle = \mid \overline{P_n(x)} \mid \; ; \; \langle l_p \rangle = \mid \overline{P_p(x)} \mid \tag{1.8}$$

where overbar indicates the expected value calculation. Different choices for the $P_i(x)$ functions would lead to different degrees of accuracy of the model and for the associated computational effort. If the $P_i(x)$ functions are taken as simple exponentials of the form

$$\begin{aligned} P_n(x) &= \begin{cases} \alpha_L e^{+\alpha_L x}, & x \leq 0 \\ 0, & x > 0 \end{cases} \\ P_p(x) &= \begin{cases} \beta_L e^{-\beta_L x}, & x \geq 0 \\ 0, & x < 0 \end{cases} \end{aligned} \tag{1.9}$$

then the LM is recovered. As we have previously shown, most of the limitations implicit in the LM arise from the fact that the dead space effect is neglected. The simplest assumption that allows to overcome such difficulty is to consider the $P_i(x)$ functions to be delayed exponentially decaying functions of the type

$$\begin{aligned} P_n(x) &= \begin{cases} \alpha_D e^{+\alpha_D (x+d_n)}, & x \leq -d_n \\ 0, & x > -d_n \end{cases} \\ P_p(x) &= \begin{cases} \beta_D e^{-\beta_D (x-d_p)}, & x \geq d_p \\ 0, & x < d_p \end{cases} \end{aligned} \tag{1.10}$$

that is, to assume that the probability of a hole (electron) initiated impact-ionization event occurring between x and $(x + dx)$ $((x - dx))$ is 0 until the carrier travels a dead space length, and $\beta_D dx$ ($\alpha_D dx$) afterwards [50]. The reason for such an assumption can be supported by the following observation. It is easily understood that the shape of the curve referred to as primary in Fig. 1.5 is proportional to $P_n(-x)$. As we see it is very close to a delayed exponential. Particularly it is possible to extract α_D and d_n from a fitting procedure. Similar arguments hold for holes. We can show that the previous assumptions, which define the DM of impact-ionization, lead to the following expressions for the generation rate [51] (see also [52] where carriers are used instead of currents)

$$\frac{dJ_p}{dx} = qG = \alpha_D J_n^H + \beta_D J_p^H = -\frac{dJ_n}{dx} \tag{1.11}$$

$$J_n^H = J_n(x + d_n) - \alpha_D \int_x^{x+d_n} J_n^H dx' \tag{1.12}$$

$$J_p^H = J_p(x - d_p) - \beta_D \int_{x-d_p}^{x} J_p^H dx' \tag{1.13}$$

Equations 1.11-1.13 are valid if impact-ionization is the only relevant generation-recombination mechanism. The appropriate boundary conditions are

$$\begin{aligned} J_p^H(x) &= 0, \ x < d_p \\ J_n^H(x) &= 0, \ x > W - d_n \\ J_p(0) &= J_{p0} \\ J_n(W) &= J_{nW} \end{aligned} \tag{1.14}$$

The DM is actually equivalent to the model developed in [50],[53] to study the mean gain of avalanche photodiodes. Equations (10-12) can be easily inserted in Drift Diffusion simulators, whose solution can still be accomplished via an iterative scheme, as proposed by Gummel [54]. Equation 1.11-1.13 have been introduced referring to constant fields, but they can be easily extended by assuming both threshold energies and impact-ionization coefficients to be dependent on the local electric field. Within the DM, the impact-ionization characteristic of a given semiconductor under a specified electric field are expressed by two pairs of parameters: the ionization coefficients and the threshold energies for electrons and holes, respectively. Those parameters are linked to the mean free path between ionizing through Eq. 1.8 which takes the form

$$\langle l_p \rangle = \frac{1}{\beta_D} + d_p \ ; \ \langle l_n \rangle = \frac{1}{\alpha_D} + d_n \tag{1.15}$$

The terms are usually negligible in the lower field range, but their contribution increases with field strength. Similar results were reported for the first time in [52] by Y. Okuto and C. R. Crowell, but up to now they have not been received considerable attention. It should be noticed that Eqs. 1.11-1.14 have been introduced referring to constant fields, but they can be easily extended by assuming both threshold energies and impact-ionization coefficients to be dependent on the local electric field.

1.2.5 Parameters extraction for Delay Model

A practical way to obtain the DM parameters is to apply general techniques of error minimization. Let us suppose that different experimental values are available, such as the multiplication factors (M_i) for electrons and holes, for a certain number of devices under a specified bias condition. First, the field shape, $F_i(x)$ corresponding to each value has to be determined. Then, a sample set of the unknown functions $(\alpha_D(F), \beta_D(F), E_{th,n}(F), E_{th,p}(F))$ is chosen, in correspondence to an arbitrary number (P) of field values, $F_h(h \in (l, P))$, and a guess is made about the range of variation of the $4P$ unknown samples $\alpha_D(F_h), \beta_D(F_h), E_{th,n}(F_h), E_{th,p}(F_h)$. The extraction procedure simply consists of two further steps: in the first we randomly choose the value of the $4P$ unknown samples in their relative range of variation. For each choice we simulate all the N structures using a suitable function to interpolate the samples, and we calculate an error function which could be just the simple mean root square of the differences between experimental and calculated $log(M_i)$ values. By tracking the sample set which gave the minimum value, we reduce the searching range and update its bound to maintain the central value over the best samples set. When the error function decreases under a prescribed quantity, the last step starts, consisting of a simple gradient search for the minimum value of the error function until the zero value is reached. A series of improvements can be thought of in order to enhance the method convergence and accuracy, depending on the particular device that furnished the experimental data. The fundamental point is that, thanks to this method, we can successfully extract a set of highly reproducible parameters that can be used to describe impact-ionization process in a given semiconductor. If we restrict our attention to structures with low overall multiplication factor ($M-1 \ll 1$), many simplifications can be done on the full DM, that allow a faster parameter extraction. We have applied the described algorithm to experimental data measured on npn $InP/In_{0.53}Ga_{0.47}As$

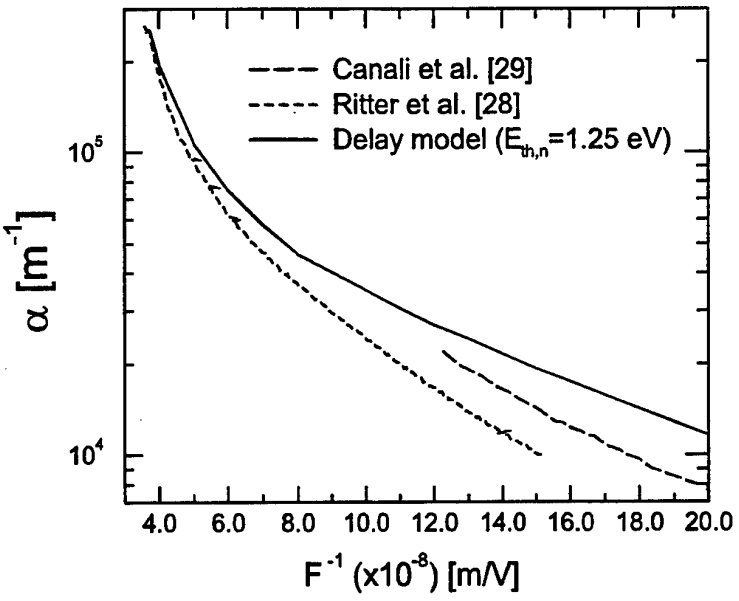

Figure 1.6: Universal DM ionization coefficient for electrons on $In_{0.53}Ga_{0.47}As$ compared with previous LM determinations. The calculated values, used in DM drift diffusion simulator, allow a perfect calculation of the multiplication factors in both HBTs.

HBTs [28, 29]. In such transistors the electron current injected from the base flows in the collector region growing because of II processes, the strength of multiplication depending on collector bias. The electron multiplication factor, M_n, is defined as the ratio between the collector current and the electron current injected from the base into the collector

$M_n = \frac{J_{n,C}}{J_{n,B}}$

With a suited procedure [29, 55] the M_n dependence on collector polarization for a given device can be extracted with great sensitivity. Both structures considered in [28, 29] are operating in the range of collector biases that satisfy the relation $M - 1 \ll 1$. For sake of simplicity we have made the widely accepted assumption to consider $E_{th,n}$ independent on the local electric field (at least for the range of fields considered). The procedure to extract an estimate of the $\alpha_D(F)$ and $d_n(F)$ functions proceeds by applying the algorithm detailed. We calculated the field shapes in the collector region for the device reported in [29] by means of a drift diffusion simulator, using doping data obtained with C-V measurements [55]. For the structure reported in [28] we referred to the nominal doping value, reported in the original work. In Fig. 1.6 we finally plot the universal electron impact ionization coefficient for $In_{0.53}Ga_{0.47}As$ extracted from our algorithm at the threshold energy of 1.25 eV (see [27]) in the considered field range. It is worth reminding that, if the LM was to be used (as actually done in [28, 29]), the ionization coefficients for the two structures would differ from one another. The calculated values on Fig. 1.6, used in DM-based drift diffusion simulator, allow a perfect calculation of the multiplication factors in both HBTs.

Chapter 2

Study of short channel effects and of hot-carrier phenomena in High Electron Mobility Transistors (HEMTs)

2.1 GaAs-based AlGaAs/InGaAs Pseudomorphic HEMT's

2.1.1 Introduction

AlGaAs/InGaAs/GaAs pseudomorphic High Electron Mobility Transistors (PM-HEMT's) have been commercially available for a few years and have proven successful in a variety of applications, including microwave and millimeter-wave low-noise amplifiers, high performance low-noise amplifiers at Q-band, and V-band monolithic power amplifiers [56, 57, 58].

Mastering hot-electron phenomena is of crucial importance for the design of power AlGaAs/InGaAs pseudomorphic HEMT's, since highly energetic carriers are responsible for on-state device breakdown, which can limit the microwave power of HEMT's [59, 60]. Hot-electrons and impact-ionization effects also negatively influence the device rf and noise behaviour [61].

Recoverable drift phenomena can derive from the trapping/detrapping of hot-electrons, and/or from the recombination of holes generated by impact-ionization with electron trapped in deep levels. In the worst case, permanent reliability problems may also arise, mostly consisting in the formation of defects or in the breaking of atomic bonds, which result in the generation of deep levels [62, 63, 64, 60, 65, 66, 67].

Spectroscopic analysis of electroluminescence (EL) has been extensively used to characterize hot carrier effects in MESFET's and HEMT's, starting from the works of Zanoni al. [68], Zappe et al. [69] and R. Ostermeir et al. [70]. In [71] we demonstrated that the dominant contribution in the electroluminescence spectrum of AlGaAs/GaAs HEMT's around the 1.4 eV region was due to recombination of electrons with holes generated by impact-ionization. We also observed, in the spectra of AlGaAs/GaAs and AlGaAs/InGaAs HEMT's [72, 73], a peak due to the band-to-band recombination of 'cold', non energetic, electrons and holes. This strongly suggested the presence of holes in the low-electric-field region of the device (gate-to-source region) [74].

Recently, N. Shigekawa, T. Enoki et al. [75, 76] were able to directly observe spatially-resolved electroluminescence at energies corresponding to direct recombination in the $In_{0.53}Ga_{0.47}As$ channel of InP-based HEMT's. By using a device having fairly large gate-source and gate-drain separations (3 μm) they demonstrated that the electroluminescence emission related to the recombination peak actually comes from the gate-source low electric field region. The authors also showed that the

photoluminescence spectra measured without applying bias voltage are identical in shape to the electroluminescence ones, a further confirm that EL is due to electron-hole recombination in the InGaAs channel.

All the experimental data summarized above confirm the results of device numerical simulations carried out in the impact-ionization regime of MESFET's or HEMT's [77, 78, 79]. Hole transport in n-channel heterojunction FET's has been studied by means of 2D drift-diffusion simulation by Kunihiro et al. [80]. Their simulation show that holes generated by impact-ionization in the high-field region near the drain travel to the source region. Due to the energy barrier at the heterointerface, the generated holes are confined to the channel layer, and accumulate near the source region as the drain voltage is increased. The accumulated holes lower the potential barrier of the source-channel junction, resulting in an increase in the drain current and output conductance. A similar bipolar effects has been described also by B. J. Van Zeghbroek et al. [81] and A. Neviani et al. [74] for MESFET's, and by Y. C. Chou et al. [82] for PM-HEMT's.

It should be stressed that this bipolar effect leads to a positive feedback mechanism possibly resulting in device breakdown (the presence of holes induces an increase in the drain current, which, in turn, leads to the generation of an increased number of holes). This could possibly explain the recent observations of burn-out occurring when a certain level of gate current is reached [9, 83]. Transport phenomena of generated holes therefore significantly contribute to the determination of breakdown effects in HEMT's.

PM-HEMT's currently adopted for power microwave amplifiers have channel lengths in the 0.1 μm $\div$ 0.3 μm range, with drain-source voltages V_{DS} which can easily exceed 5 V. At these bias levels, extremely high electric fields are present in the gate-drain access region, and significant hot-carrier phenomena have been observed, such as infrared and visible light emission and the increase in negative gate current I_G, due to holes generated by impact-ionization and collected at the gate electrode [84, 73]. All these effects demonstrate the presence of highly energetic carriers which can trigger device breakdown or degradation.

Previously reported failure modes consist in (a) recoverable increase in drain current due to compensation of negative trapped charge by holes generated by impact-ionization [63]; (b) development of electron traps in the gate-to-drain access region, inducing a permanent decrease in I_D and the so-called "breakdown walkout", i.e. an increase in the breakdown voltage of the gate-drain Schottky diode [64, 60]; (c) increase in the density of interface states present at the AlGaAs/InGaAs heterointerface due to hot carrier stressing, resulting in catastrophic I_D decrease [65].

In this part of the report we analyze carrier transport phenomena occurring in pseudomorphic AlGaAs/InGaAs HEMT's biased in the on-state impact-ionization regime. In particular: (i) we confirm the presence, in the electroluminescence spectra of pseudomorphic HEMT's, of a dominant contribution due to electron-hole recombination, and we identify a composite peak due to recombination of cold carriers; (ii) we analyze the recombination peak using a high-resolution monochromator, which reveals the fine structure due to transitions between electron and hole subbands in the channel quantum well, thus providing useful data concerning the properties of the InGaAs HEMT channel. This kind of information is the same available from photoluminescence spectra, but can be obtained directly on production HEMT's in operating conditions; (iii) by means of high resolution spectral analysis and spatially-resolved electroluminescence micrographs we demonstrate that recombination between non-energetic electrons and holes occurs in the gate-source region, as observed by N. Shigekawa et al. [75] for InAlAs/InGaAs HEMT's on InP. This recombination emission is superimposed to a less intense contribution mostly coming from the gate-drain region. This contribution has a nearly maxwellian distribution which extends to fairly high energies ($>$ 3 eV) and has equivalent temperatures in the 1000 - 3000 K range; (iv) we also show that at high V_{DS} and electric field, significant recombination occurs in the AlGaAs layers, which demonstrates the real space transfer of both electrons and holes.

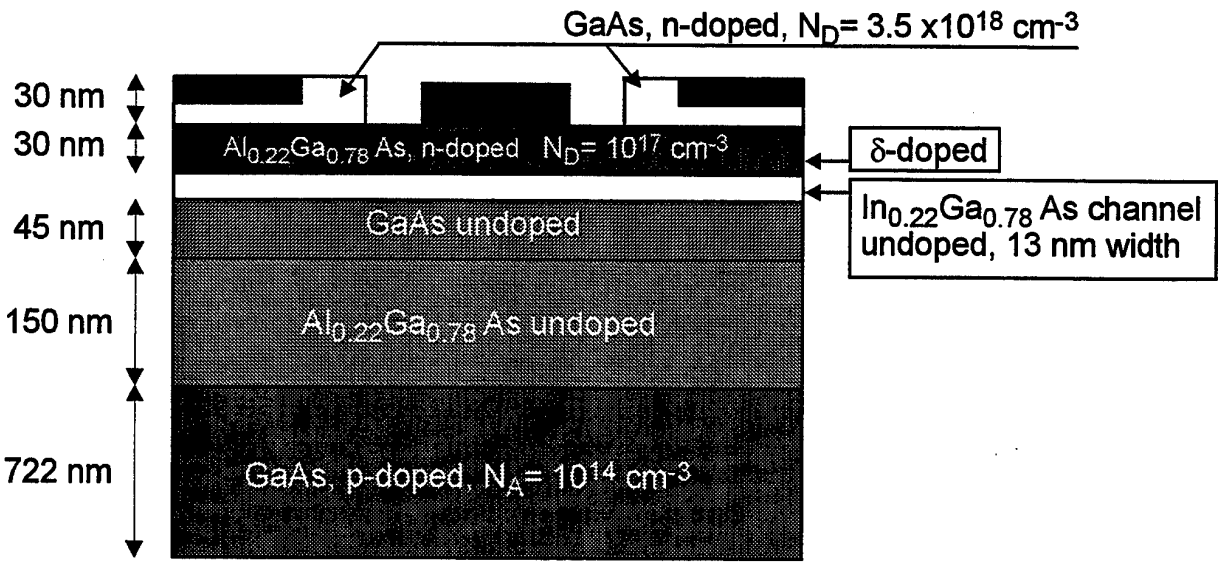

Figure 2.1: Schematic representation of the simulated device

We also report on a new failure mechanism of AlGaAs/InGaAs PM-HEMT's, which has been observed after hot carriers DC accelerated tests. Indeed, a permanent degradation has been found, consisting in the decrease of drain current and of the absolute value of the pinch-off voltage $|V_p|$ at low V_{DS}. DC, pulsed and low-frequency AC analyses, current Deep Level Transient Spectroscopy (DLTS) and photoinjection measurements demonstrate that the failure mechanism consists in the creation of deep levels under the gate which act as electron traps at low gate-to-drain electric fields.

2.1.2 Short channel effects in PM-HEMTs

This part of the report is dedicated to the study of short channel effects in PM-HEMTs on GaAs. We focus mainly on the high speed performance of such devices when the gate length has nanometer dimensions.

Performance enhancements of high electron mobility transistors (HEMT) are mainly achieved by scaling down the device gate length using high resolution electron beam lithography. Improvements of such characteristics as gate capacitance, transconductance and transit frequency are expected and they should be connected with high nonstationariety in short devices: most electrons are traveling through the gate-controlled active zone without suffering any scattering, or suffering very few. Under these conditions of ballistic transport, one can reach very high drift velocities, much higher than stationary ones.

In order to study quantitatively the short channel effects on drift velocity and transit frequency of a pseudomorphic HEMT, two devices with different gate lengths have been studied using our self consistent many particle ensemble Monte Carlo (MC) simulator. A three valley nonparabolic band structure is used for each consistent material. The electron trajectories are traced in two dimensions in real space subject to all the principal scattering agent. Polar optical phonon, deformation potential and impurity scattering mechanisms are present, as well as the action of the self consistent two dimensional electric field profile. The MC procedure is coupled with a two dimensional Poisson solver. Transport of holes and impact ionization are not taken into account in this study. All simulations assume room temperature operations.

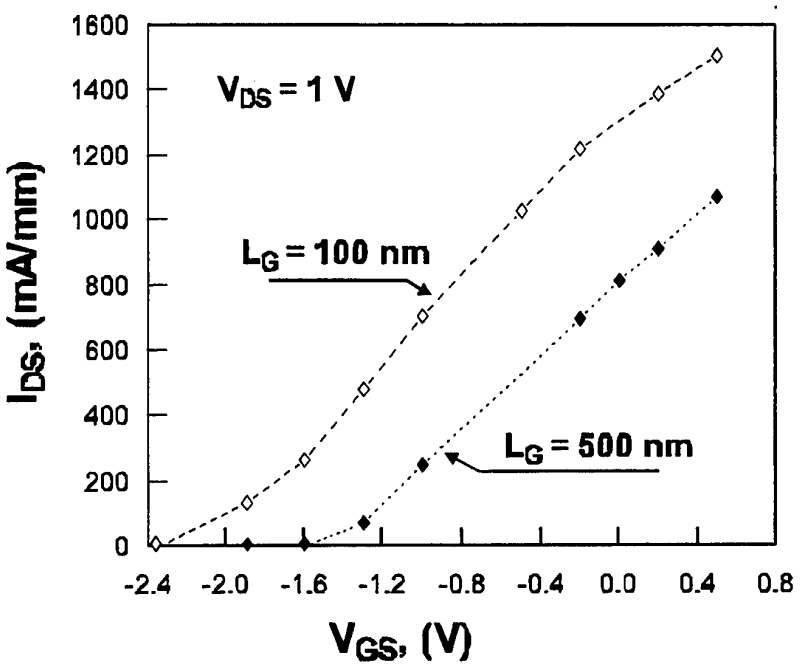

Figure 2.2: Calculated transfer characteristic for the two simulated devices.

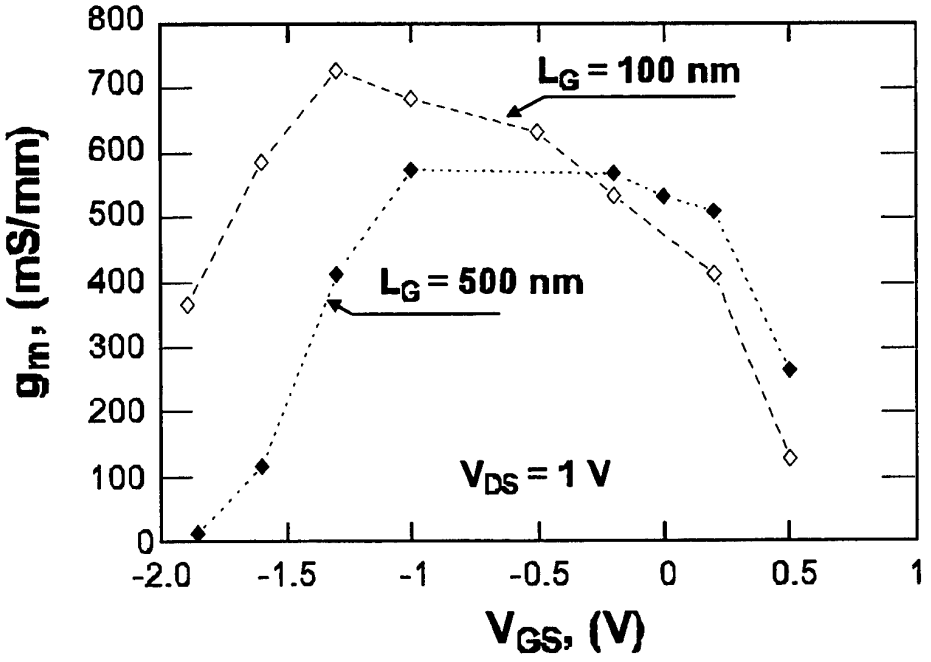

Figure 2.3: Calculated transconductance for the two simulated devices.

The simulated devices are schematically presented in Fig. 2.1. The level of δ-doping of the AlGaAs donor layer is $N_d = 5 \cdot 10^{12} cm^{-2}$. The regions under the source and drain contacts are intensively doped down to the middle of the channel, in order to provide the highest possible carrier density in the channel. The source-gate (L_{SG}) and gate-drain (L_{GD}) lengths are equal for both devices ($L_{SG} = L_{GD} = 200$nm), while the gate length (L_G) changes: the short device has $L_G = 100$ nm and the long one $L_G = 500$ nm.

The calculated transfer characteristics for both devices are shown in Fig. 2.2. Drain current decreases with gate length increases. In the current saturation region at high gate voltages the ratio of

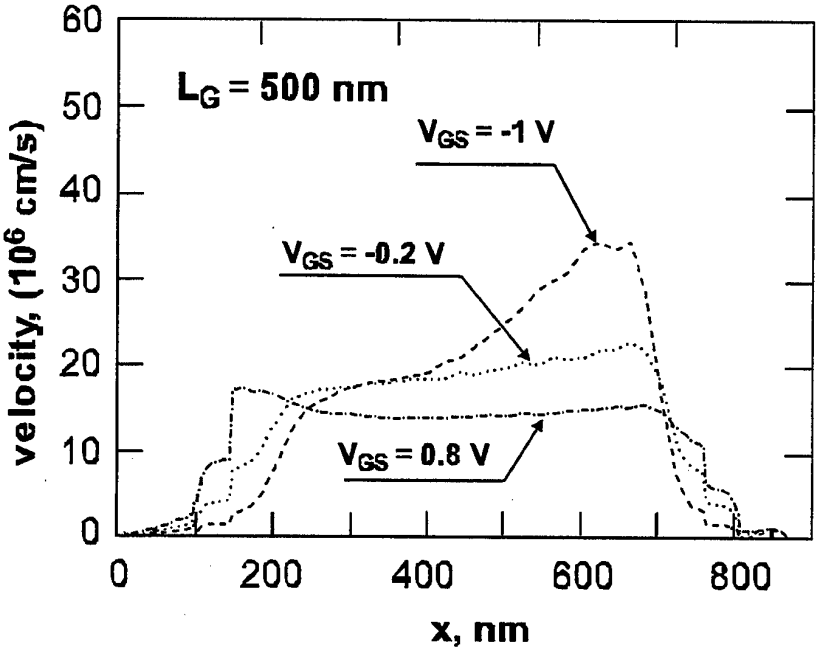

Figure 2.4: Electron velocity averaged in y-direction as a function of the distance along the device for the a channel length of 500 nm measured at V_{DS} = 1 V. x-axis is along channel length, y-axis is perpendicular to the channel.

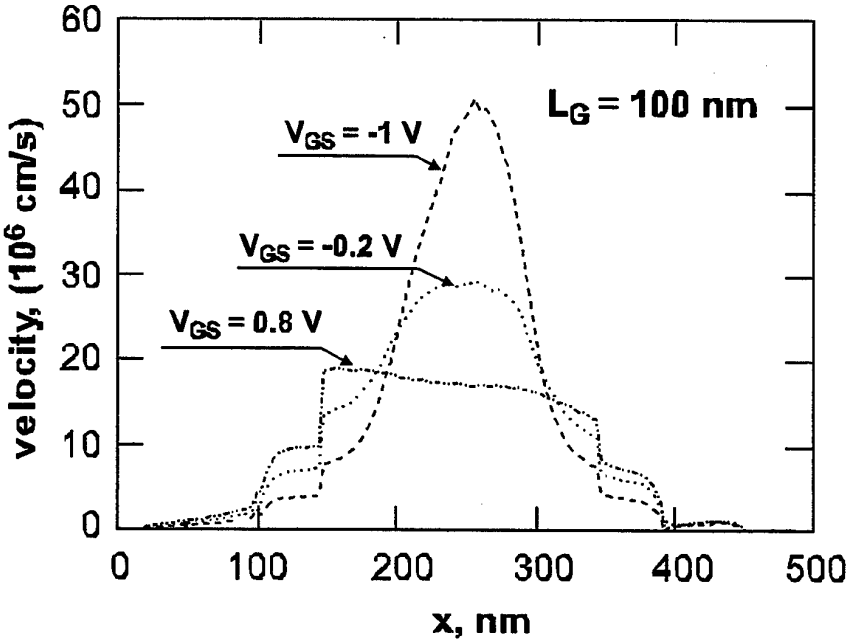

Figure 2.5: Electron velocity averaged in y-direction as a function of the distance along the device for the a channel length of 100 nm measured at V_{DS} = 1 V. x-axis is along channel length, y-axis is perpendicular to the channel.

drain current in two devices under consideration is only 1.5. One can see (Fig. 2.3) that the maximum transconductance is larger for the smaller device, as expected by the theory [85]. The shorter gate length device tends to loose the transconductance more rapidly when the gate voltages V_{GS} exceed -0.5 V, thus achieving values comparable to those of the larger device. This is due to both real-space

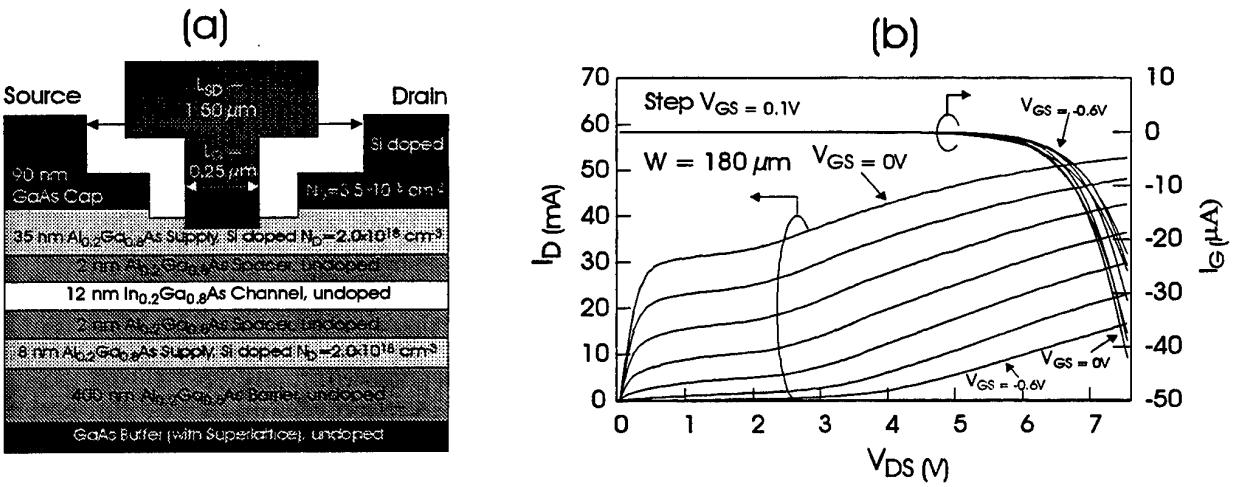

Figure 2.6: **(a)** Schematic cross section of the 0.25 μm gate length PM-HEMT devices. **(b)** Drain, I_D, and gate current, I_G, as a function of V_{DS} at different values of V_{GS} (V_{GS} = -0.6 V to 0 V, step 0.1 V).

transfer of electron in the parasitic AlGaAs channel and to the more substantial reduction of gate capacitance (CG) at high gate voltages, caused by lower quantity of carriers in shorter gate length device [85].

In Figs. 2.4 and 2.5 the electron velocity averaged in y-direction is plotted as a function of the distance along the device for the 500 nm and 100 nm gate length devices, respectively. The peak of the velocity in the end of gate region is 1.4 times more pronounced for 100 nm gate length device, but the line shape seems to be the same for both HEMTs. The figures clearly show the presence of the ballistic transport of particles at short gate length device, since the average velocity at low gate voltages exceeds the drift velocity in conventional materials at least 1.5 times.

2.1.3 Samples description and experimental apparatus

Tested devices were fabricated by MBE, with the structure shown in Fig. 2.6(a). From top to bottom the layer sequence consists of a highly doped GaAs cap layer, a 35 nm $Al_{0.2}Ga_{0.8}As$ upper barrier layer with an active Si doping concentration of about $N_D = 2 \cdot 10^{18} cm^{-3}$, a 2 nm undoped $Al_{0.2}Ga_{0.8}As$ upper spacer layer, a 12 nm $In_{0.2}Ga_{0.8}As$ undoped channel layer, a 2 nm undoped $Al_{0.2}Ga_{0.8}As$ lower spacer layer, a 400 nm $Al_{0.2}Ga_{0.8}As$ lower barrier layer on a GaAs buffer (with superlattice) followed by the semi-insulating GaAs substrate. The $Al_{0.2}Ga_{0.8}As$ barrier layer below the channel contains an 8 nm thick doping layer with an active doping concentration of about $N_D = 2 \cdot 10^{18}$ cm^{-3}. A T-shaped, recessed gate with gate length $L_g = 0.25$ μm was adopted. Source-to-drain distance, L_{SD}, measured from contact edges is 1.5μm; gate width, W, was varied from 80 μm to 240 μm. To avoid metal/semiconductor interdiffusion effects, a refractory metal-interdiffusion barrier was chosen for the gate metallization. Alloyed AuGeNi contacts were used for source and drain. Devices were passivated using SiN. Typical devices have a maximum drain current I_{DSAT}/W = 450 mA/mm; the value of drain saturation current measured at V_{DS} = 2 V, V_{GS} = 0 V is I_D = 170 mA/mm. The maximum transconductance, measured at V_{DS} = 2 V, V_{GS} = 0 V is g_{mMAX} = 400 mS/mm. Typical cut-off frequency, f_T, of these devices is about 50 GHz.

Electrical measurements have been carried out by means of a Hewlett-Packard 4155 Semiconductor Parameter Analyzer. Great care has been taken to avoid oscillations during DC measurements. Measurements as a function of temperature have been carried out in a temperature-controlled chamber.

Optical measurements have been obtained using the apparatus described in [72]. The devices were

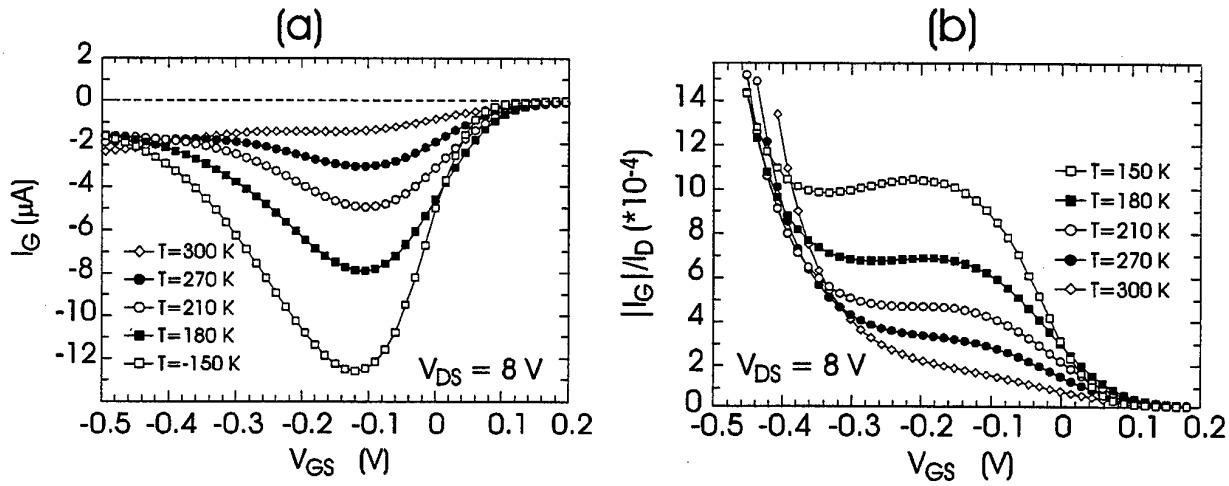

Figure 2.7: **(a)** I_G vs V_{GS} at high V_{DS} (V_{DS} = 8 V). **(b)** $|I_G|/I_D$ vs V_{GS} merasured at different temperatures, T.

assembled in a temperature controlled chamber and the emitted light was collected through an optical fiber (3 mm in diameter) placed about 1 mm away from the device. Two monochromators have been used; the first, suitable for low-resolution, wide range spectroscopic analysis has a resolution of 0.02 eV; the other one allows high resolution spectra to be measured (bandwidth less than 0.003 eV). The spectra analysis of the emitted photons was carried out using the monochromators and two single-photon-counting photomultipliers suitably cooled in order to improve the signal to noise ratio. The photomultipliers used are: 1. EMI 9684 (S1 response) and 2. EMI 9816 (S20 response) and cover the spectral range from 1.1 eV to 6 eV. After an amplitude selection the pulses at the output of the photomultipliers were shaped using a constant fraction discriminator (ORTEC 583) and were sent to a counter (ORTEC 776) driven by a computer.

2.1.4 Electrical measurements

Figure 2.6(b) shows the output characteristics of a W = 180 μm device at room temperature. A remarkable increase in the (negative) gate current I_G takes place for $V_{DS} > 4$ V. When the devices under test are biased at high V_{DS}, due to the high electric field present in the gate-drain region, significant hot-electron phenomena take place. In particular, electrons can reach energies high enough to create electron-hole pairs by impact-ionization. Impact-ionization rate can be evaluated by measuring the negative (outgoing) gate current, I_G, which is due to the holes generated by impact-ionization and collected at the gate electrode. The kink observed in the output I-V characteristics is possibly due to the onset of impact-ionization, which causes hole pile-up at the source, compensating negative charge trapped in the gate recess region, as it will be explained in Section II.

The bell-shaped behaviour of I_G as a function of V_{GS} is the typical signature of impact-ionization, see Fig. 2.7(a). In the impact ionization regime the behaviour of I_G as a function of the gate voltage V_{GS} at constant V_{DS} is non-monothonic, as reported in Fig. 2.7(a). Starting from pinch-off, $|I_G|$ first increases as V_{GS} increases, due to the increasing in the drain current and consequently in the number of high-energetic electrons in the channel; then it decreases, as V_{GS} further increases, due to the lowering of the gate-drain electric field and, consequently, of the electron energy [86]. When the temperature is lowered, electrons undergo a reduced phonon scattering thus achieving higher energies. As a consequence the impact ionization rate increases giving rise to a higher gate current, see Fig. 2.7(a).

As it has been shown by K. Hui et al. [87] in an n-channel FET structure the $|I_G|/I_D$ ratio is

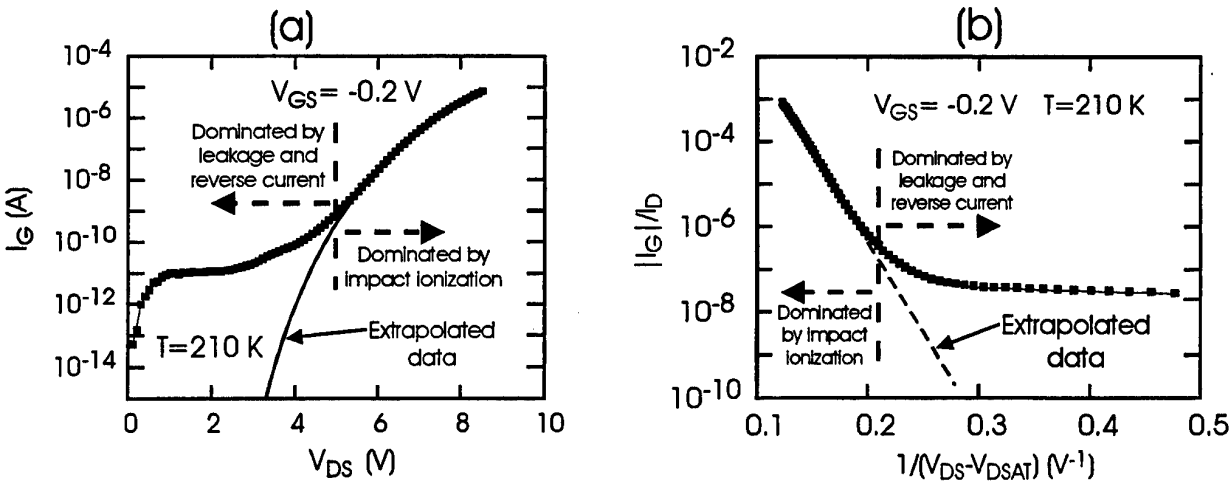

Figure 2.8: **a)** $|I_G|$ vs. V_{DS} in semi-logarithmic scale measured at V_{GS} = -0.2 V and at 210 K. The continuous line represents the extrapolated data, obtained from Fig.2.8(b), and indicates the hole induced gate current that should be detected in absence of leakage. **b)** $|I_G|/I_D$ vs $1/(V_{DS} - V_{DSsat})$ measured at V_{GS} = -0.2 V and at 210 K. The exponential dependence observed at high V_{DS} confirms the impact ionization model and allows us to extrapolate (continuous line) the $|I_G|/I_D$ ratio at low V_{DS} where the leakage is dominant.

proportional to the $\alpha_n \cdot L_{eff}$ product, where α_n is the electron impact-ionization coefficient of the channel material, and L_{eff} is the extension of the channel region where impact-ionization takes place:

$$|I_G|/I_D \simeq \alpha_n \cdot L_{eff} \simeq L_{eff} \cdot exp\left(-\frac{1}{E}\right) \simeq L_{eff} \cdot exp\left(\frac{-L_{eff}}{V_{DS} - V_{DSsat}}\right) \tag{2.1}$$

E is the longitudinal electric field in the L_{eff} region and V_{DSAT} is the drain saturation voltage.

In Fig. 2.7(b) the gate current to drain current ratio I_G/I_D is shown. For V_{GS} < -0.3 V the reverse current of the gate-drain Schottky junction dominates I_G; the device is pinched-off and the drain current is decreasing as V_{GS} is pushed towards negative values. This explains the increase in I_G/I_D going from -0.3 V to -0.5 V in Fig. 2.7(b). For -0.3 V < V_{GS} < -0.1 V impact-ionization dominates I_G, and the I_G/I_D ratio is almost constant. For V_{GS} > -0.1 V the decrease in the gate-drain electric field, together with the temperature increase (due to the increase in power dissipation) and the possible transfer of electrons to the AlGaAs layer contribute to lower the impact-ionization rate down to very low values. At decreasing the temperature, the gate current and the multiplication ratio increase due to the reduced phonon scattering and improved electron transport properties, which lead to more energetic electrons.

Figure 2.8(a) shows the gate current in semilogarithmic scale as a function of V_{DS} for V_{GS} = -0.2 V and T = -60 °C. The plateau at low V_{DS} (V_{DS} < 3 V) in Fig. 2.8(a) is related to the gate diode leakage and reverse current. The reverse current decreases at low temperature. At 210 K, the reverse current at V_{GD} = - 2 V is approximately 10 pA, which demonstrates the good quality of the gate Schottky junction.

According to Eq. 2.1, by plotting in a semi-logarithmic scale $|I_G|/I_D$ versus $1/(V_{DS} - V_{DSAT})$, a straight line is obtained, see Fig. 2.8b, which allows one to extrapolate the $|I_G|/I_D$ curve down to low V_{DS} values, thus obtaining an indication of the V_{DS} value ($\simeq$3 V) which marks the onset of impact ionization, see continuous lines in Figs.2.8(a) and (b).

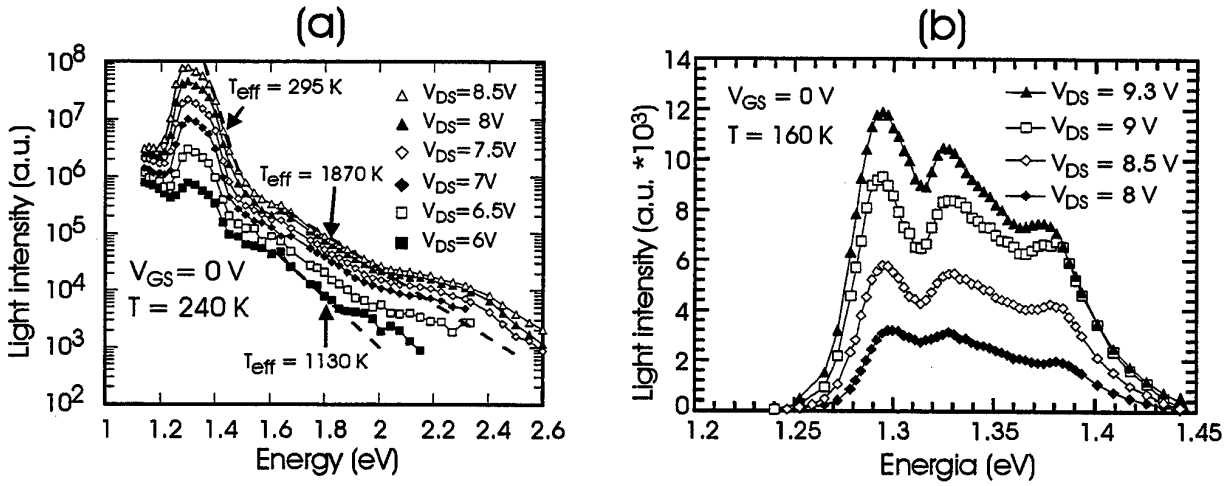

Figure 2.9: **(a)** Emitted light intensity as a function of energy at T = 240 K for various V_{DS} and at V_{GS} = 0 V. **(b)** Recombination peak spectra, evaluated with an higher resolution system for different V_{DS} (at V_{GS} = 0 V, T=160 K).

2.1.5 Electroluminescence measurements

The electroluminescence radiation emitted by the devices under test, biased at high V_{DS}, was analyzed in the 1.1 - 2.6 eV range. Figure 2.9(a) shows electroluminescence spectra taken at 240 K in a device biased at V_{GS} = 0 V from V_{DS} = 6 V to V_{DS} = 8.5 V. As it has been already observed for PM-HEMT's [84], the spectra consists of a nearly-exponential component, of a broad peak in the 1.2 - 1.4 eV region, and of a high-energy tail at energies larger than 2 eV.

We measured the average logarithmic slopes of the central portion of the spectra, which are approximately maxwellian. In the following, will refer to this values as 'equivalent temperatures', T_{eq}, of the photon energy distribution. It should be stressed that these equivalent temperatures are used only with the aim of comparing the relative 'heating' of the photon distribution in the various bias conditions. In fact, it has already been demonstrated for Si MOSFETs that there is no direct correspondence between this photon equivalent temperature and the effective temperature of the carrier energy distribution [88].

The equivalent temperatures increase from 1100 K at V_{DS} = 6 V to 1900 K at V_{DS} = 8.5 V.

In order to better appreciate the various components of the peak centered around 1.35 eV, we analyzed it at an higher energy resolution (at T = 160 K), see Fig. 2.9(b). Three different peaks have been identified, plus a possible fourth one, which appears as a "shoulder" at 1.35 eV. The shape of the recombination peak does not change significantly at increasing the drain-source voltage, see Fig. 2.9(b). Only the intensity increases, again following the increase in the impact-ionization current.

The peak centered around 1.35 eV has been analyzed also as a function of temperature, see Fig. 2.10(a). Electroluminescence peaks can be better resolved at low temperature; for temperatures higher than 195 K, thermal quenching possibly occurs [89], and the highest energy peak disappears, see Fig. 2.10(a).

Since the depth of the $In_{0.2}Ga_{0.8}As$ channel layer is 120 Å, quantization of energy levels occurs, as previously observed [11, 90]. We therefore attributed the peaks in Fig. 2.9(b) and in Fig. 2.10(a) to radiative recombination between conduction and valence subbands in the InGaAs quantum well, [91, 84, 92]. Due to the strong band bending which occurs in the device under bias, the parity selection rules between envelope functions vanish in these devices, leading to the observation of radiative recombination between conduction band sub-level C2 and heavy-hole sub-level HH1. The energy of the peaks shifts toward higher values as the temperature is decreased. Figure 2.10(b) shows the shift of

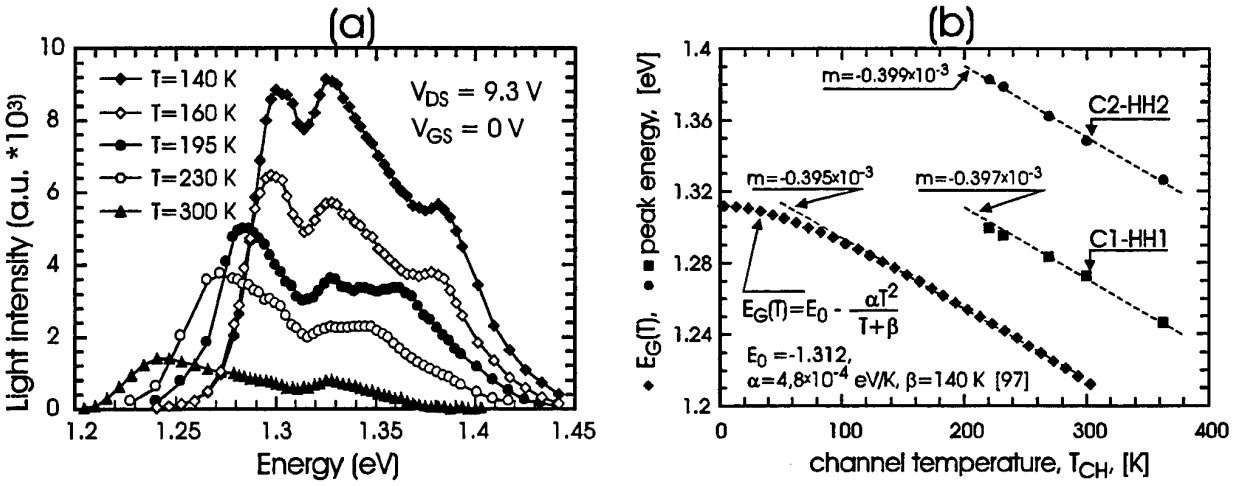

Figure 2.10: **(a)** Recombination peak spectra, evaluated with the higher resolution system, measured at V_{DS} = 9.3 V, V_{GS} = 0 V at different temperatures. **(b)** Peak energy position (C1-HH1 and C2-HH2) and energy gap variation of $In_{0.21}Ga_{0.79}As$ as a function of channel temperature. The good correlation between the slopes is well visible.

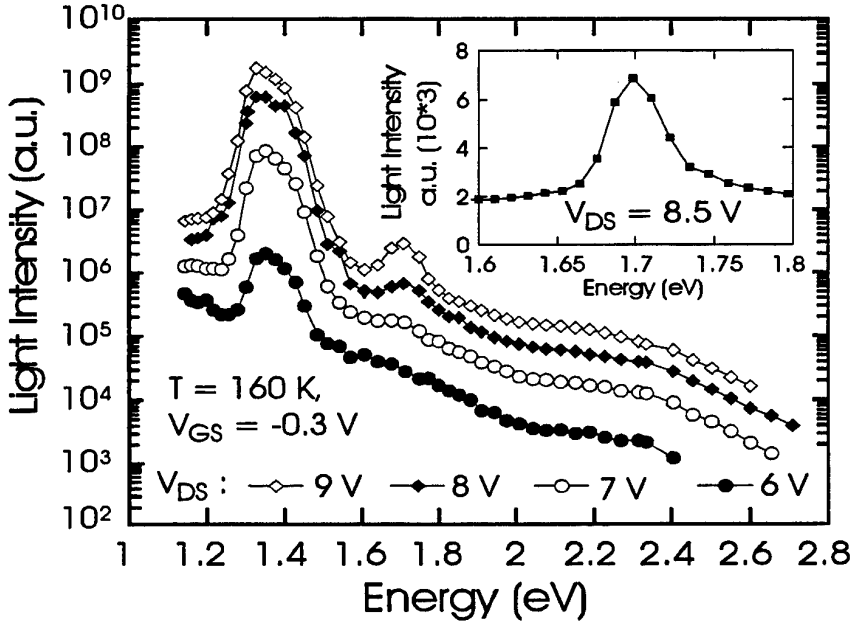

Figure 2.11: Emitted light intensity as a function of energy at T = 160 K for various V_{DS} and at V_{GS} = -0.3 V. The peak at 1.7 eV measured with an higher resolution system at V_{DS} = 8.5 V is depicted in the inset.

the energy of the C1-HH1 and C2-HH2 peaks as a function of temperature, corresponding to a linear coefficient of approximately -0.4 meV/K. The behavior of peak energy as a function of temperature is compared to that of the energy gap of $In_{0.2}Ga_{0.8}As$, as reported in [93]. The intensity of the peak also increases at decreasing the temperature, following the corresponding increase in I_G, see Fig.2.10(a).

The shape of the recombination peak does not change significantly at increasing the drain-source voltage, see Fig.2.9(b). Only the intensity increases, again following the increase in the impact-ionization current.

Beyond V_{DS} = 8 V a peak at $\simeq$ 1.7 eV appears, Fig. 2.11, which corresponds to band-to-band recombination in $Al_{0.2}Ga_{0.8}As$.

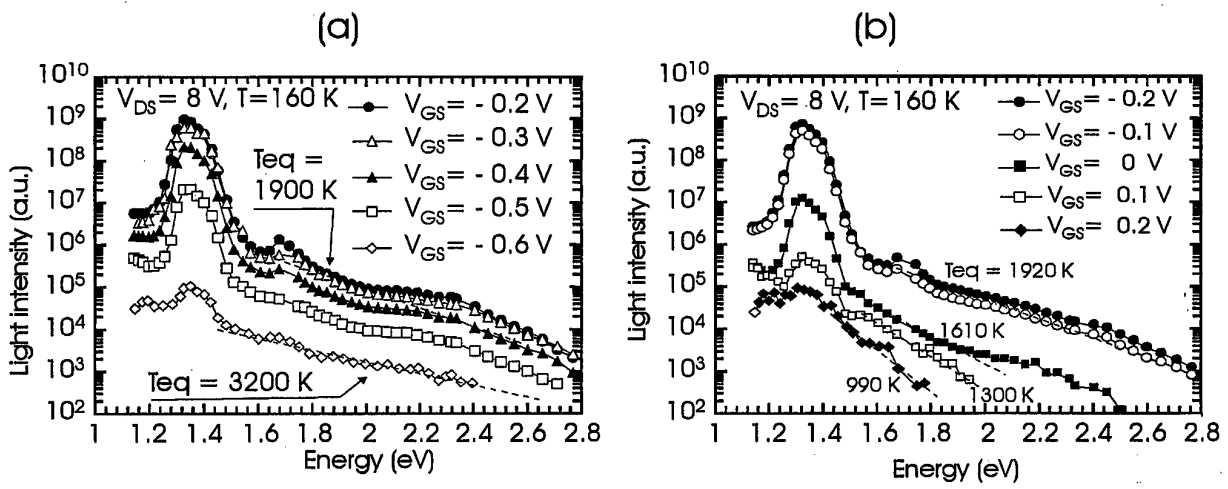

Figure 2.12: Emitted light intensity as a function of energy at T = 160 K at V_{DS} = 8 V for various V_{GS}: a) $-0.6V < V_{GS} < -0.2V$ b) $-0.2V < V_{GS} < +0.2V$.

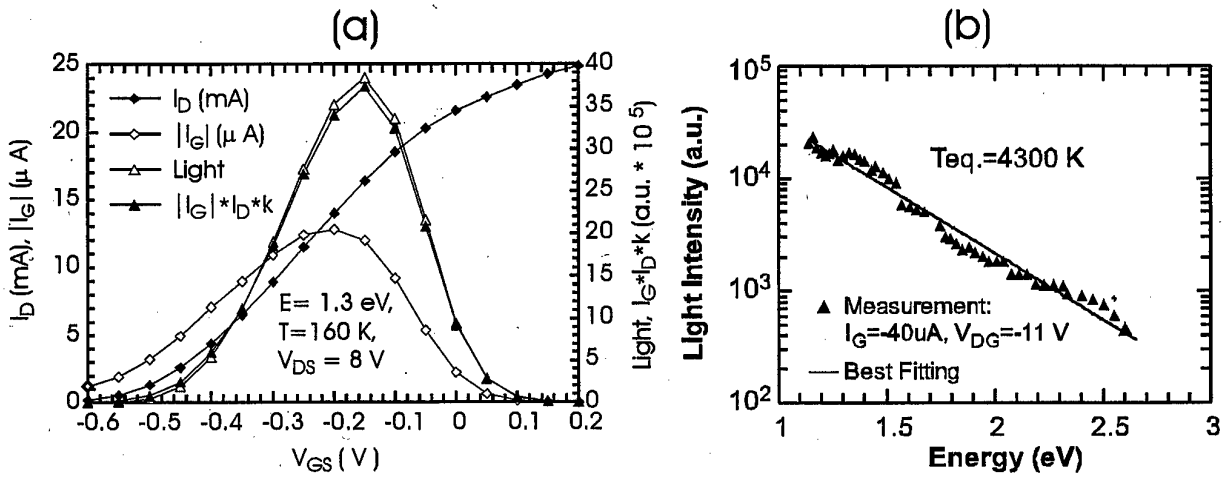

Figure 2.13: **(a)** I_D, $|I_G|$, $I_G \cdot I_D$ and 1.3 eV light emitted as a function of V_{GS}, measured at V_{DS} = 8 V, T=160 K. **(b)** Emitted light intensity as a function of energy emitted by the gate-drain device section (source floating) biased at a constant reverse current $I_{GD} = -40\mu A$. T = 4300 K.

The intensity and the shape of the emitted spectra markedly depend on V_{GS}, see Figs. 2.12(a) and (b) and Fig. 2.13(a). The behavior of the intensity of the emitted radiation is non monotonic, and drops below the sensitivity of the detection system for V_{GS} < -0.6 V and V_{GS} > 0.2 V, despite I_D is monotonically increasing as V_{GS} is increased from pinch-off to positive values. On increasing V_{GS} the gate-drain electric field decreases, leading to a decrease in the electron energy; as a consequence, the equivalent temperature of the high energy photon distribution decreases from T= 3200 K at V_{GS} = -0.6 V to T = 1000 K at V_{GS}= +0.2 V, following the corresponding decrease in I_G/I_D, see Fig. 3(b). Impact ionization also decreases, and the electron-hole recombination peak disappears.

Figure 2.13(a) compares the 1.3 eV radiation intensity with gate current I_G, drain current I_D, and their product $I_G \cdot I_D$, all measured as a function of V_{GS} at T = 160 K, with V_{DS} = 8 V. An astonishing correlation between the electroluminescence intensity at 1.3 eV and the $I_G \cdot I_D$ currents product is obtained.

The electroluminescence spectra obtained in the on-state conditions have been compared to the spectrum measured when only the gate-drain junction is reverse biased at a constant gate current,

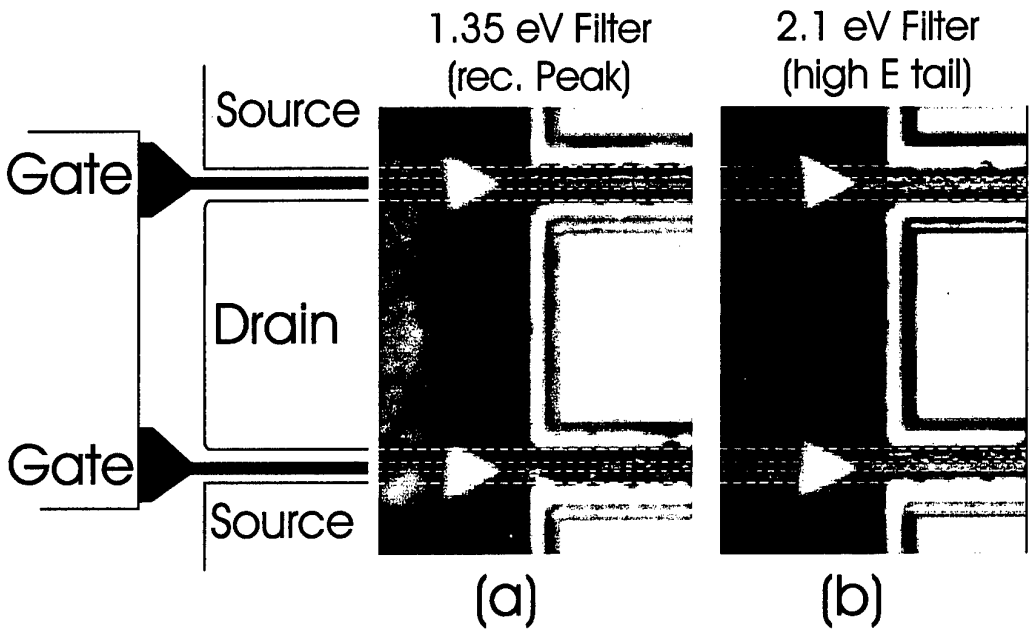

Figure 2.14: False-color emission microscopy images taken in on-channel conditions in correspondence of the maximum negative gate current (maximum impact-ionization), at V_{DS} = 8.5 V and V_{GS} = -0.3 V, RT. Left, **(a)** , micrograph taken through a 1.35 eV bandpass filter (recombination peak): the emission is located between gate and source. Right, **(b)** , bandpass filter at 2.1 eV (hot carriers); emission occurs between gate and drain.

with a value of $I_G \simeq 40\mu A$, corresponding to the one measured in the open channel conditions (In this condition $V_{DG} \simeq -11$ V). In this bias conditions, only the electrons which are injected from the gate due to field-assisted thermionic emission are able to impact-ionize, so that a much higher electric field value between gate and drain is needed to sustain the same I_G as in on-state conditions. As a consequence, the equivalent temperature observed is much higher than in on-state, i.e. T_{eq} = 4300 K, see Fig. 2.13(b). Moreover, in these bias conditions, the recombination peak completely disappears.

The spatial distribution of the emitted radiation was observed by means of an Hamamatsu Phemos P200 emission microscopy system. Several micrographs were taken with different applied bias, both in the on-state and in the off-state conditions. For all bias conditions the emission was evenly distributed along the gate fingers, and no current filamentation or preferential breakdown point was observed.

In order to identify the origin of the various spectral components, micrographs were taken through band-pass filters. The bias conditions corresponding to the maximum gate current and light intensity were chosen, i.e. V_{GS} = -0.3 V at V_{DS} = 8.5 V. To locate the site of the emission of recombination peaks we adopted a bandpass filter centered at 1.35 eV; the sensitivity of the microscope detection system was reduced, so that the imaging system was actually capable of detecting only the high intensity peaks. Despite the gate dimension of 0.25 μm is close to the optical resolution of the microscope, we can notice that recombination emission at 1.35 eV clearly comes from the gate-source access region, see Fig. 2.14(a). Another micrograph was taken using a bandpass filter at 2.1 eV, i.e. in the high energy tail of the spectra, and the maximum detector sensitivity. As it is shown in Fig. 2.14(a), no emission is detected between gate and source, and all the signal is collected between gate and drain. Of course, if we keep the sensitivity of the detector at the maximum level, we can observe this emission between gate and drain also at 1.3 eV. By comparing the spectra taken with the HEMT in saturation, Figs. 2.9(a), 2.11, and 2.12, with those taken when only the gate-drain Schottky contact and heterojunction

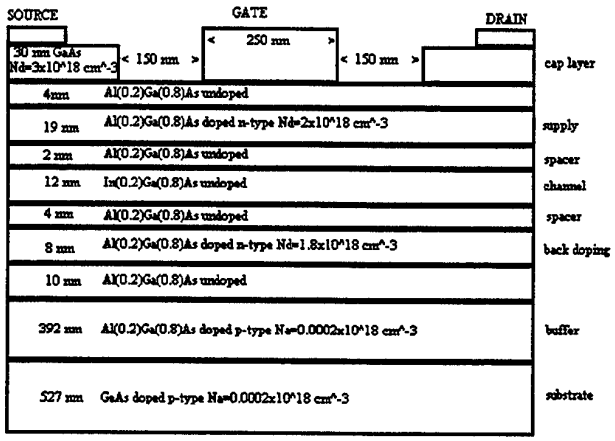

Figure 2.15: Schematic representation of the simulated device

(source floating)is reverse biased, Fig. 12, we can conclude that the electroluminescence spectra of pseudomorphic HEMTs are due to the superimposition of two components: (i) a continuous 'hot carrier' emission, extending from the infrared to the visible region; (ii) isolated recombination peaks. The former is related to the presence of hot carriers in the high field gate-drain region of the devices, and is responsible also for the emission in two-terminal breakdown conditions, Fig. 2.13(b). The latter contribution comes from the low field gate-source region, and is present only in the three-terminals saturation bias conditions, see Figs. 2.9(a), 2.11, and 2.12.

2.1.6 Simulation of the impact ionization and electroluminescence in PM-HEMTs

We have previously applied our MC simulation to the study of short channel effects in PM-HEMTs. There we deliberately neglected impact ionization. We present now the results of the simulation when impact ionization is accounted for, and the dynamics of the impact-generated holes is followed in parallel to the electron one. The presence of electrons and holes in the InGaAs channel open the way for radiative recombination processes leading to band edge electroluminescence. We show that the MC results can be used in conjunction with a Tight Binding approach to effectively calculate electroluminescence spectra which agree well with experimental results.

The structure of the simulated HEMT is shown in Fig. 2.15. The gate length is 250 nm. A double heterostructure (AlGaAs/InGaAs/AlGaAs) is present, that guarantees better electron confinement in the channel. Delta doping is used in the upper as well as in the lower barrier. Ohmic contacts are simulated by two highly doped regions that penetrate from source and drain pads directly into the channel region. No channel quantization has been considered.

Figure 2.16(a) shows the simulated transfer characteristics of the device (at t = 20 ps). The simulated structure correspond to the test devices described in the previous section. The HEMT switches off with a bias V_{GS} of -0.9 V. In Fig. 2.16(b) we see that, for values of V_{DS} higher than 3 V,

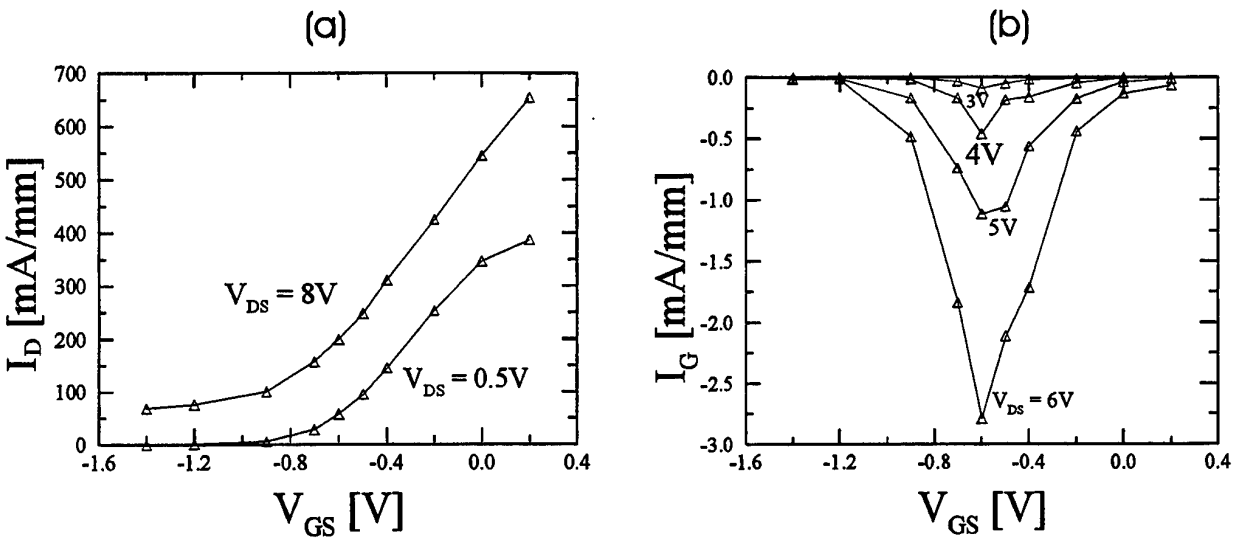

Figure 2.16: **a** Transfer characteristics of the device, as obtained from Monte Carlo simulations at t = 20 ps. **b** Simulated gate current as a function of the gate bias for several drain bias, t = 20 ps.

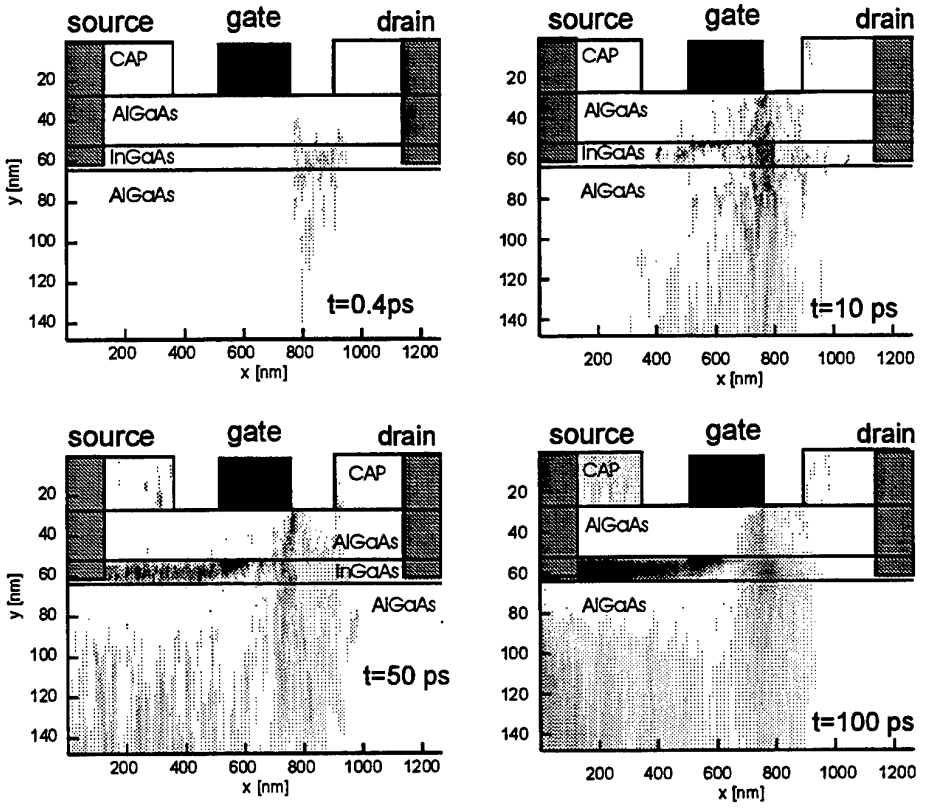

Figure 2.17: Representation of the transport dynamics of holes generated by impact-ionization. At t=0 the impact ionization processes are switched-on.

a negative current (about two orders of magnitude lower than the drain current) is collected at the gate. Such current is due to those holes that are generated in the high field region of the channel and travel toward the gate. A larger number of holes do actually move back towards the source contact, accumulating near the source contact region.

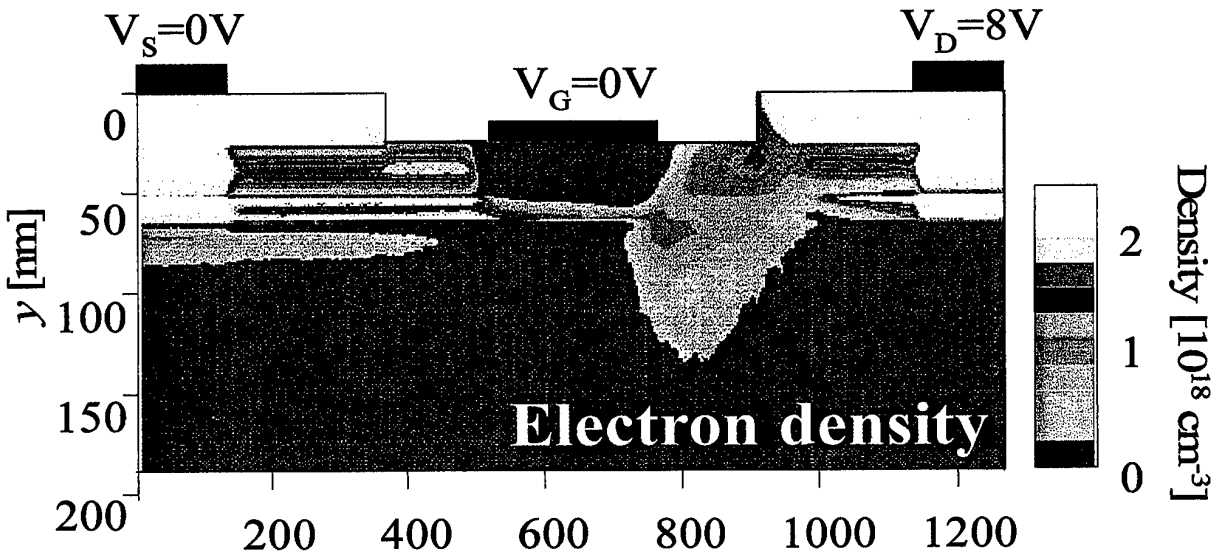

Figure 2.18: Electron density in the simulated HEMT, at V_{DS}= 8 V, V_{GS}= 0 V, t = 20 ps.

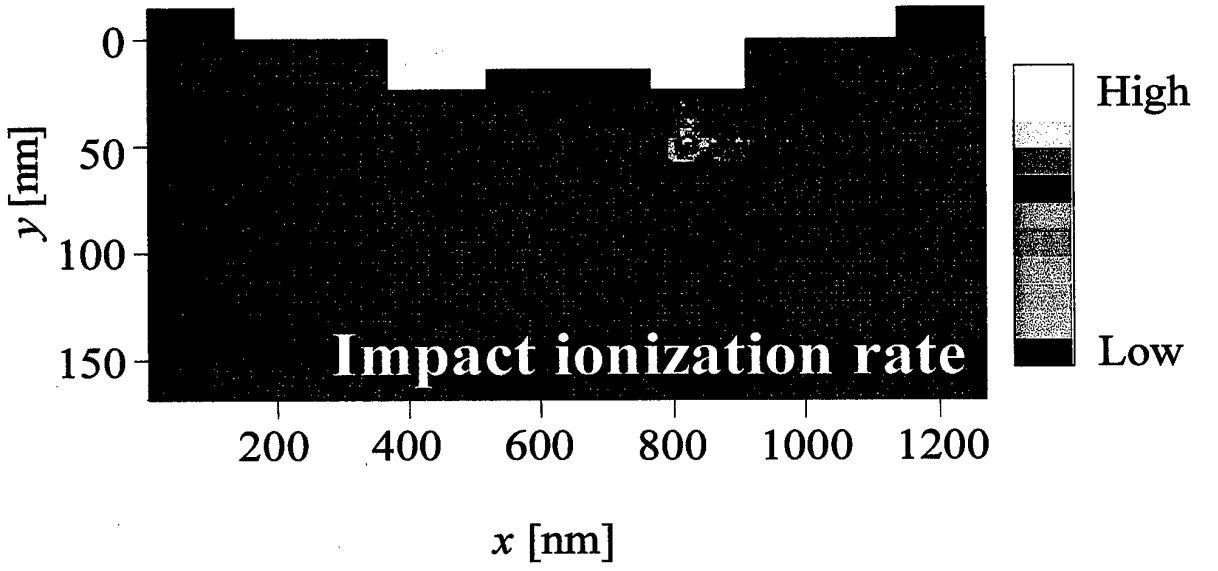

Figure 2.19: Impact ionization rate in the simulated HEMT, at V_{DS}= 8 V, V_{GS}= 0 V, t = 20 ps.

The gate current displays a maximum as a function of V_{GS} as already observed and discussed in the 2.1.4 section.

In figures 2.17 the dynamics of the generated hole is followed for a bias condition of V_{GS} = -0.2 V and V_{DS} = 8 V. Time zero correspond to the stationary simulation performed without impact ionization. At this time the ionization processes is turned on. At short times (400 fs) we can see that holes are generated at the gate end of the channel, in correspondence to the high fied region where electrons are very hot. After 5-10 ps, holes are moving towards gate and source contacts. At longer times (30-50 ps) holes reach the source contact region and accumulate there, thus creating a condition for direct electron-hole radiative recombination. Injection of holes in the top and bottom AlGaAs layers is also clearly visible.

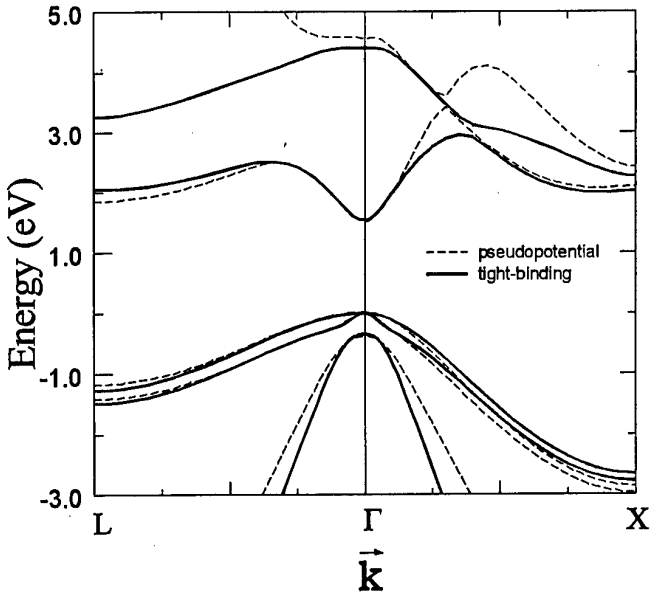

Figure 2.20: Comparison between tight–binding band structure and non–local empirical pseudopotential band structure of GaAs at 0 K

2.1.7 Monte Carlo simulation of electroluminescence effects in PM-HEMT's

Under bias conditions close to the breakdown of the device, the electrons gain energy from the high-field gate to drain region and are able to move to upper valleys. Since in the upper valleys the effective mass is higher, the electrons lose velocity and consequently the carrier density increases as shown in Fig. 2.18. At the same time, since the potential energy is higher than the electron's energy gap, electrons are able to generate holes via the impact ionization process.

Figure 2.19 shows the simulated impact-ionization rate in the tested HEMT (the device structure is shown in Fig. 2.16) biased at V_{DS}= 8 V, V_{GS}= 0 V. As expected, electron-hole generation mostly occurs in the InGaAs channel, in the gate-drain region, where the electrons reach their maximum energy. Some ionization events also occur in the top AlGaAs layer in the same device region, see Fig. 2.19. The generated hole radiatively recombine with electrons. In order to calculate the HEMT electroluminescence we have developed a tight-binding (TB) approach. This allows us to describe electronic and optical properties of nanostructure devices beyond the usual envelope function approximation and to account for strain, band non-parabolicity, and indirect band gap at the same time. The band structure obtained within the TB approach compared with a pseudopotential result is given in Fig. 2.20.

Optical properties within the tight-binding approach are obtained by using a recent theory proposed by M. Graf and P. Vogl [94] which allows one to calculate those properties without introducing new fitting parameters.

By using the distribution function as obtained by the MC simulation and the TB calculation we are able to calculate the electroluminescence spectra of the HEMT. The calculated electroluminescence spectra, for T = 195 K, as a function of the emission energy are shown in Fig. 2.21 (bottom), together with the hole density (top). The picture shows the accumulation of holes under the gate and in the gate-source region. Indeed, holes created in the gate-drain region are sweeped back from the electric field and reach the gate-drain region where they stops since the electric field is quite low. The electroluminescence is high close to the gate and decreases moving in the source direction. Moreover, the electroluminescence is composed by a broad peak around 1.3 eV ad two other minor peaks close to 1.35 eV. In order to clarify the electroluminescence spectrum we show in Fig. 2.22

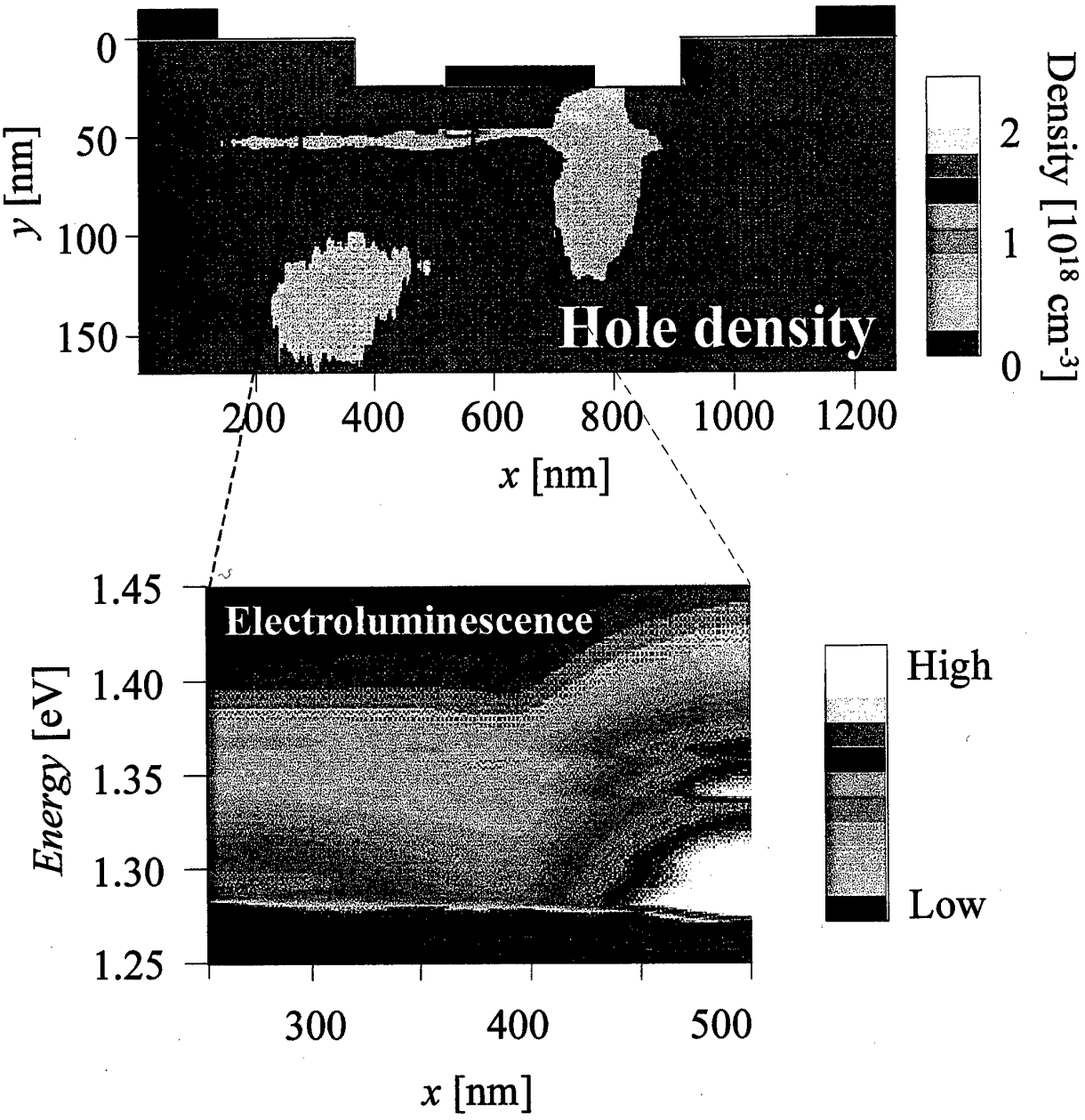

Figure 2.21: Hole density and electroluminescence spectra in the simulated HEMT, V_{DS}= 8 V, V_{GS}= 0 V, t=20 ps,. The spectra are taken at a depth y = 50 nm (inside the InGaAs channel) and at various position x along the channel. Recombination peaks occur at x=450 ÷ 500 nm.

the electroluminescence spectrum as a function of emission energy for a given channel position. A comparison with available experimental results is given.

We observe that the bias induced bending of the quantum well forming the channel allows radiative recombinations of electrons and holes even from levels normally forbidden under flat band condition. Indeed, as shown in Fig. 2.23 , the C2 → HH1 transition is forbidden for a symmetric quantum well, but becomes allowed when the well is distorted by the band bending (see Fig. 2.24) Furthermore, we observed that the emitted light is mainly polarized in the in-plane direction since the levels have essentially a heavy-hole character.

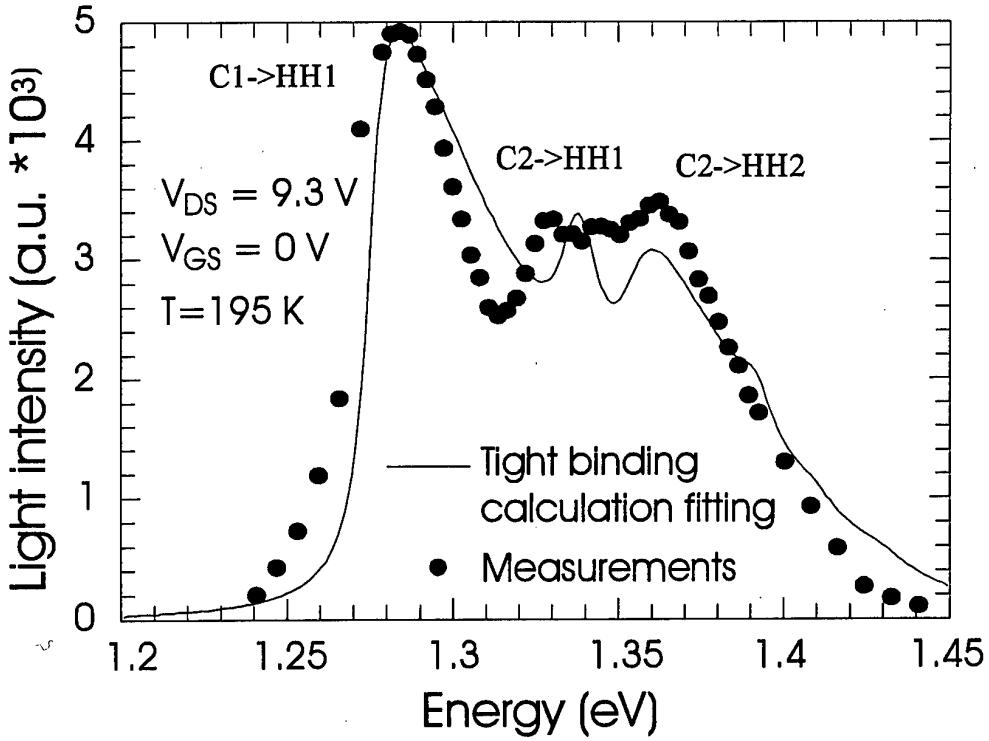

Figure 2.22: Comparison between calculated and measured electroluminescence spectra

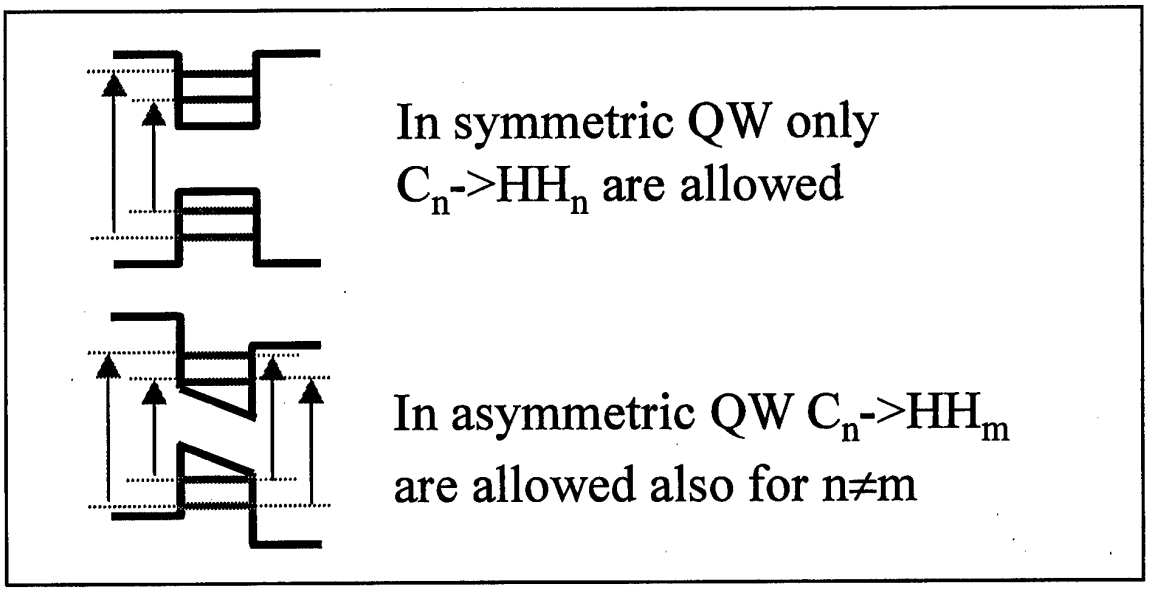

Figure 2.23: Selection rules

2.1.8 Discussion and Conclusions

We have shown in Figs. 2.9(a), 2.11, and 2.12 that the on-state electroluminescence signal emitted by HEMTs in saturation region consists, in the 1.1 eV - 3.1 eV energy range, of a series of peaks in the 1.25 - 1.45 eV region, of a peak at 1.7 eV, followed by a central part having a nearly Maxwellian behaviour and by a long high-energy tail extending well beyond 2 eV. We start our discussion with the analysis of the high-energy portion of the spectra. Photons with energies larger than 1.45 eV are emitted from the gate-drain region of the device, where the longitudinal electric field and carrier

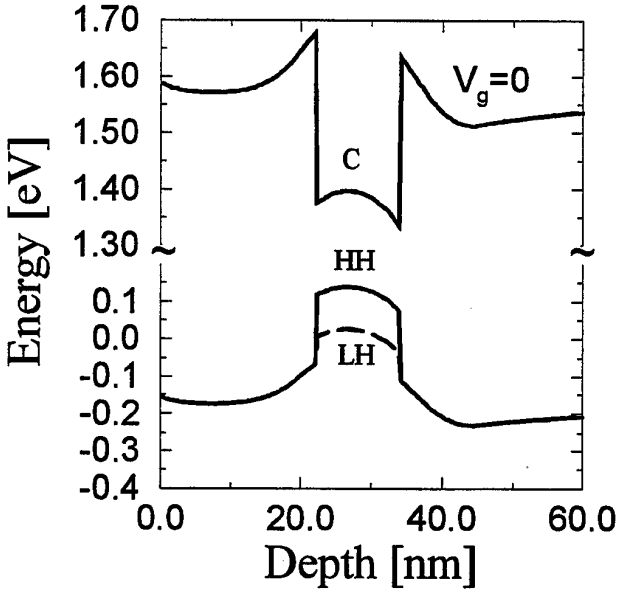

Figure 2.24: Band edge profile of the HEMT channel

energies are at their maximum. As a consequence, the intensity and equivalent temperature of this photon distribution closely follow the dependence of electric field on V_{DS} and V_{GS}, i.e. they increase at increasing V_{DS}, see Fig. 2.9(a), and decrease at increasing V_{GS}, see Figs. 2.12(a) and (b), with the same behaviour of the multiplication ratio I_G/I_D. Measurements of electroluminescence in this spectral region therefore provide a reliable and noninvasive monitor of hot carrier transport phenomena in submicrometer HEMTs.

Light emission in the gate-drain region is accompanied by remarkable carrier multiplication effects due to impact-ionization. Holes, generated by impact-ionization, are accelerated by the intense electric field present in the gate-drain region. Part of them overcome the AlGaAs/InGaAs barrier and are collected by the gate contact, thus originating the negative gate current. Part remain in the channel and travel towards the source as also demonstrated by Monte Carlo simulation.

At very high V_{DS}, simultaneous real space transfer of electrons and holes occurs, leading to carrier transport in the AlGaAs layer, which is confirmed by the appearance of a recombination peak corresponding to the energy gap of $Al_{0.2}Ga_{0.8}As$.

Most of the holes, however, remain in the InGaAs channel, where they lose their energy and recombine with 'cold' electrons in the gate-source region, thus giving rise to recombination peaks whose energies correspond to the transitions between the different sub-band levels in the quantized InGaAs channel layer.

The high resolution analysis of the electroluminescence spectra allows one to obtain data concerning the layers structure and integrity. These data have also been confirmed by tight binding calculation fitting. The type of information which is provided by high-resolution electroluminescence is the same as in the case of the photoluminescence technique, but can be carried out on completed devices in operating conditions, and does not require flat wafers or special test structures.

Emission microscopy and Monte Carlo simulation clearly demonstrates that recombination between cold carriers occurs at the source end of the channel, Figs. 2.14 and 2.17, as already observed by Shigekawa et al. in InAlAs/InGaAs HEMTs on InP [75, 76].

The parasitic bipolar effect due to the presence of positive charge in the gate-source channel and channel/buffer regions can give rise to a positive feedback mechanism eventually leading to device breakdown and burn-out in on-state conditions (the positive charge enhances electron injection in the

channel at the source end, and this electron current at his turn enhances hole generation by impact-ionization at the drain end). This may explain why on-state breakdown voltage can be significantly lower than drain-source off-state value [83].

In conclusions, we have carried out a series of new electroluminescence measurements in pseudomorphic HEMT's biased in the 'hot-carrier' regime. The presented data, beside confirming the capabilities of electroluminescence spectroscopy and microscopy for the analysis of hot carrier effects in submicrometer devices, demonstrate the importance of taking into account hole transport and the related parasitic bipolar effects in the modeling and evaluation of on-state breakdown of pseudomorphic HEMT's.

2.2 InP-based $In_{0.53}Ga_{0.47}As$ HEMTs (lattice-matched on InP)

2.2.1 Summary

InAlAs/InGaAs/InP High Electron Mobility Transistors "InP-based" (HEMTs) have demonstrated excellent high-frequency and low-noise performances. The application of these devices to power millimeter wave systems, however, is limited by the enhanced impact-ionization effects which take place in the narrow-bandgap InGaAs channel. Enhanced impact-ionization effects have a number of negative consequences, such as reduced off-state [95, 96, 97] and on-state [98, 83, 11, 9] breakdown voltages, increase in output conductance and kink effects [99, 100], permanent device degradation [9, 101].

In particular, recent work [83, 9] has underlined the relevance of on-state breakdown voltage in determining device power and reliability [102]. On-state breakdown is determined by impact-ionization in the InGaAs channel [98, 11, 75, 76].

Several approaches to enhance the breakdown voltage of InP-based HEMTs have been adopted. Enoki proposed a composite channel combining a thin layer of $In_{0.53}Ga_{0.47}As$ and InP as the channel material [103]. With this structure, it is possible to exploit the advantageous physical properties of both materials, i.e. the high electron mobility of $In_{0.53}Ga_{0.47}As$ at low electric fields, and the high breakdown and saturation velocity of InP at high electric fields [104, 105].

Another approach to improve the breakdown voltage is to reduce the thickness of the $In_{0.53}Ga_{0.47}As$ channel to the order of the de Broglie wavelength, which makes it possible to enhance the effective bandgap in the channel due to quantum size effects (channel quantization). Channel quantization is believed to emerge as a promising approach for exploiting the excellent transport properties of $In_{0.53}Ga_{0.47}As$ [106].

In this work we employ both approaches described above to improve the breakdown voltage. We present a detailed study of the on- and off-state breakdown behaviour of $In_{0.53}Ga_{0.47}As$ InP composite-channel HEMTs with a variable $In_{0.53}Ga_{0.47}As$ layer thickness of 30 Å, 50 Å and 100 Å. Our results strongly suggest that by reducing the $In_{0.53}Ga_{0.47}As$ layer thickness, and consequently increasing the effective channel bandgap, both on- and off-state breakdown phenomena in these InP-based HEMTs can be optimized without compromising device performances.

2.2.2 Device Description and DC characteristics

To study the effect of channel quantization on breakdown in InGaAs/InP composite-channel HEMTs, a basic device structure was designed. The only variable design-parameter was the thickness of the InGaAs channel, varied as 30 Å, 50 Å and 100 Å, while keeping the other layers unchanged. A schematic of the InGaAs/InP composite channel HEMT employed in our study is shown in Fig. 2.25(a). All heterostructures were grown by MBE on a semi-insulating InP-substrate. From bottom to top, the basic structure consists of an $In_{0.52}Al_{0.48}As$ buffer layer, a 100 Å InP layer doped $2 \cdot 10^{18} cm^{-3}$ followed by a 50 Å undoped InP layer, which acts both as a spacer layer and a channel. Then, a $In_{0.53}Ga_{0.47}As$ channel with a variable thickness of 30 Å, 50 Å and 100 Å was grown, followed by a 15 Å spacer layer and a 50 Å Si-doped ($8 \cdot 10^{18}\text{cm}^{-3}$) $In_{0.52}Al_{0.48}As$ donor layer. Finally, a 250 Å undoped $In_{0.40}Al_{0.60}As$ Schottky layer was grown, followed by a 70 Å doped ($5 \cdot 10^{18}\text{cm}^{-3}$) $In_{0.53}Ga_{0.47}As$ cap layer. In the resulting structure the conduction electrons are confined within the channel and essentially form a two-dimensional electron gas. The increased Al content of the $In_{0.4}Al_{0.6}As$ Schottky layer has been chosen aiming at increasing the gate Schottky barrier height, thus improving the gate-drain diode breakdown voltage [107].

Reducing the channel thickness to values comparable to the de Broglie wavelength of the electrons causes some phenomena related to the wave-particle duality of the electron to become evident. One of these phenomena is the quantization of the electronic states in the channel in the direction per-

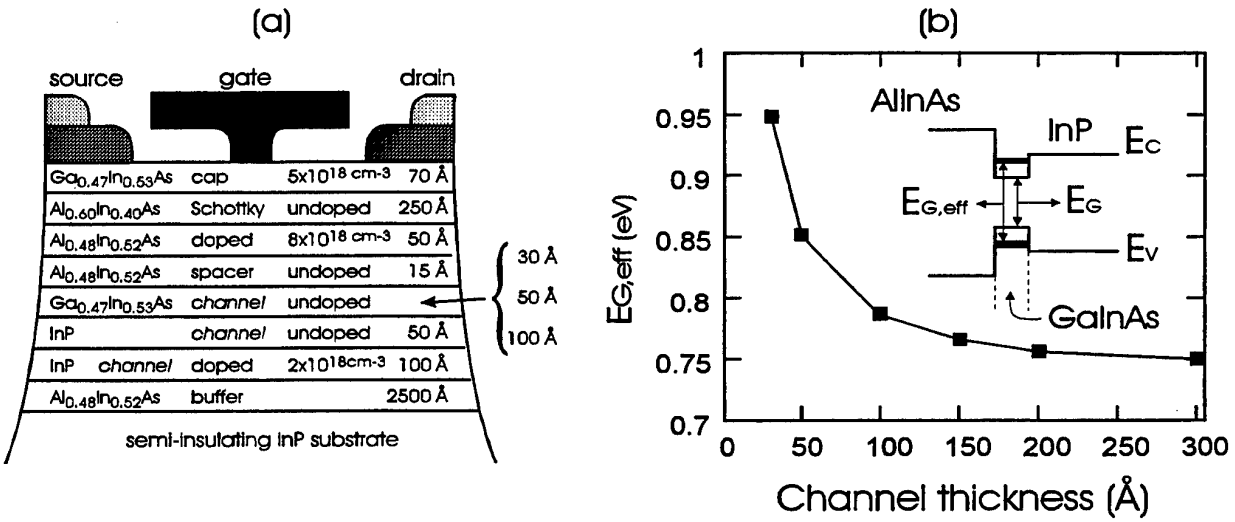

Figure 2.25: (a) Schematic cross-section of the basic InAlAs/InGaAs/InP composite-channel HEMT. (b) Effective energy-gap $E_{G,eff}$ as a function of channel thickness, calculated solving the Schrödinger equation in flat band conditions (square well approximation).

pendicular to the heterointerface plane [90]. The resulting discrete energy levels can be calculated by self-consistently solving the Schrödinger and Poisson equations, as shown in [104], where devices with InGaAs/InP composite channel structure similar to our devices were studied. The main result is that, at low electric fields (under the source end of the gate) most of the electrons are confined in the low energy gap, InGaAs channel, while at high electric fields (under the drain end of the gate) most of the electrons are located in the InP sub-channel [104].

Channel quantization also results in increased effective energy gap $E_{G,eff}$, which can be defined as the difference between the first quantized energy levels in the conduction and in the valence band. The relation between $E_{G,eff}$ and the channel thickness is depicted in Fig. 2.25(b), which was obtained by solving the Schrödinger equation alone (that is, in flat band condition). Due to this approximation, the result might be inaccurate, but it is useful to demonstrate that $E_{G,eff}$ increases when the channel thickness is reduced.

Sheet charge densities and electron mobilities have been characterized using Hall measurements at 25 °C (see Table 1). Both the sheet electron density and the mobility decrease with decreasing channel thickness. HEMTs with 0.15 μm gate lengths and drain-to-source spacings of 2 μm were fabricated for all three layer structures with variable $In_{0.53}Ga_{0.47}As$ channel thickness. Electrical characterization of the devices was done using a HP4145 semiconductor analyzer.

The DC current-voltage characteristics (at $V_{GS} = 0$ V) of the 30 Å, 50 Å and 100 Å devices are shown in Fig. 2.26(a). Transconductance measurements (at $V_{DS} = 1.2$ V) are shown in Fig. 2.26(b).

Table 2.1: Electronic properties and typical device characteristic values of $Ga_{0.47}In_{0.53}As$/InP composite-channel HEMTs with variable $Ga_{0.47}In_{0.53}As$ channel thickness

$In_{0.53}Ga_{0.47}As$ channel thickness (Å)	electron density n_s (cm^{-2})	electron mobility μ_e (cm^2/Vs)	V_P(V) V_{DS}= 100 mV	I_{DSS}(mA/mm) V_{GS}= 0 V V_{DS}= 1.5 V	$g_{m,peak}$ (mS/mm) V_{DS}= 1.2 V
30	3.7 10^{12}	7000	-0.6	283	456
50	3.9 10^{12}	9000	-0.7	427	685
100	4.2 10^{12}	9100	-0.7	551	850

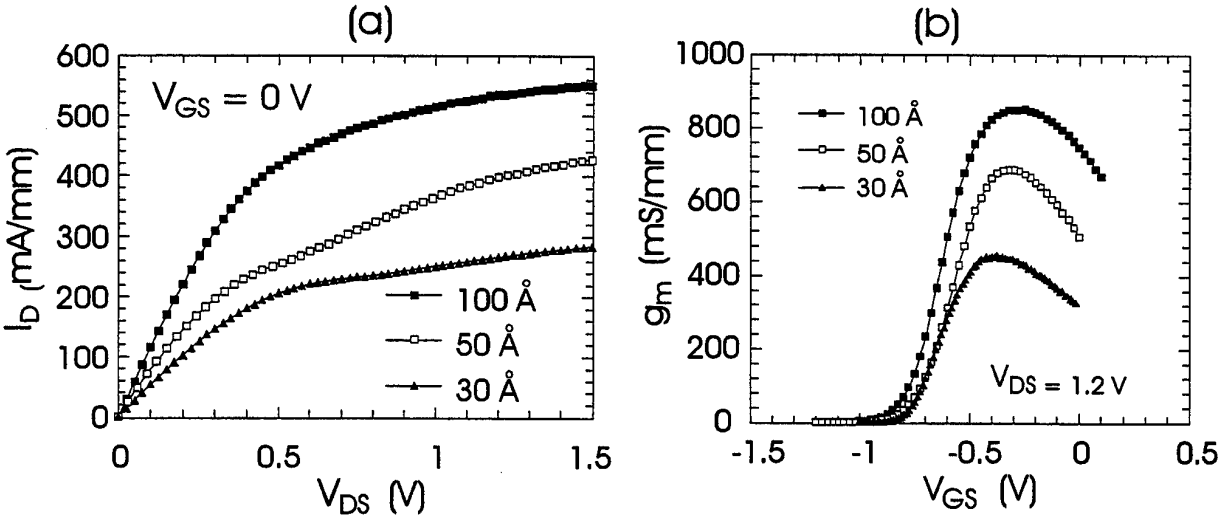

Figure 2.26: Drain Current vs V_{DS} (measured at V_{GS} = 0 V) **(a)**, and Transconductance vs. V_{GS} (measured at V_{DS} = 1.2V) **(b)**, of composite-channel HEMTs with different $In_{0.53}Ga_{0.47}As$ channel thickness: 30 Å, 50 Å and 100 Å.

Estimates of typical device characteristics, including the pinch-off voltage V_P, the channel current I_D, and the maximum transconductance, $g_{m,peak}$, are listed in Table 2.1. The variations in sheet charge density and electron mobility of the 30 Å, 50 Å and 100 Å devices are clearly reflected by the differences in transconductance and the full channel current density. With decreasing InGaAs channel thickness, the DC device performance is reduced, however, the performance of all these HEMTs is still fairly good.

2.2.3 Impact Ionization vs channel thickness

On-State Breakdown Characteristics

On-state breakdown effects in the HEMTs have been evaluated by measuring the gate current I_G as a function of the gate-source voltage V_{GS} in saturation (V_{DS} = 1.8 V). In this experiment the source contact is grounded. Fig. 2.27 shows the gate current measurements of our composite-channel HEMTs for the different $In_{0.53}Ga_{0.47}As$ channel thicknesses (30 Å, 50 Å and 100 Å). The typical "bell-shaped" behaviour observed in Fig. 2.27(a) is related to the occurrence of impact ionization in the channel [108]. This impact ionization effect is observable at a drain-source voltage as low as V_{DS} = 1.8 V. While the effect is small in the 30 Å channel HEMT, it is much more pronounced for the 50 Å and the 100 Å channel devices. To compare the magnitude of the ionization effect in the different devices, we consider the multiplication ratio I_G/I_D, which is proportional to the electron impact ionization rate α [87, 109].

Figure 2.27(b) shows the behavior $|I_G|/I_D$ as a function of V_{GS}. For all devices, the ratio I_G/I_D decreases with increasing V_{GS} (towards positive values), due to the reduction in the electric field [108]. However, the magnitude of I_G/I_D, increases substantially when comparing consecutively the 30 Å, 50 Å and 100 Å channel devices.

By defining the on-state breakdown voltage at which the gate current normalized to the gate width I_G/W reaches 1 mA/mm, we obtain a typical value of 7 V for devices with 30 Å $In_{0.53}Ga_{0.47}As$channel, and 4 V for 100 Å $In_{0.53}Ga_{0.47}As$ channel devices, both evaluated at V_{GS} = -0.4 V, which is close to the peak of I_G vs V_{GS} curve. This definition of open channel breakdown is consistent with the finding that the open channel burn-out voltage at a fixed V_{GS} occurs when the multiplication current due to impact ionization (to which the gate current I_G is proportional) reaches a certain level [9].

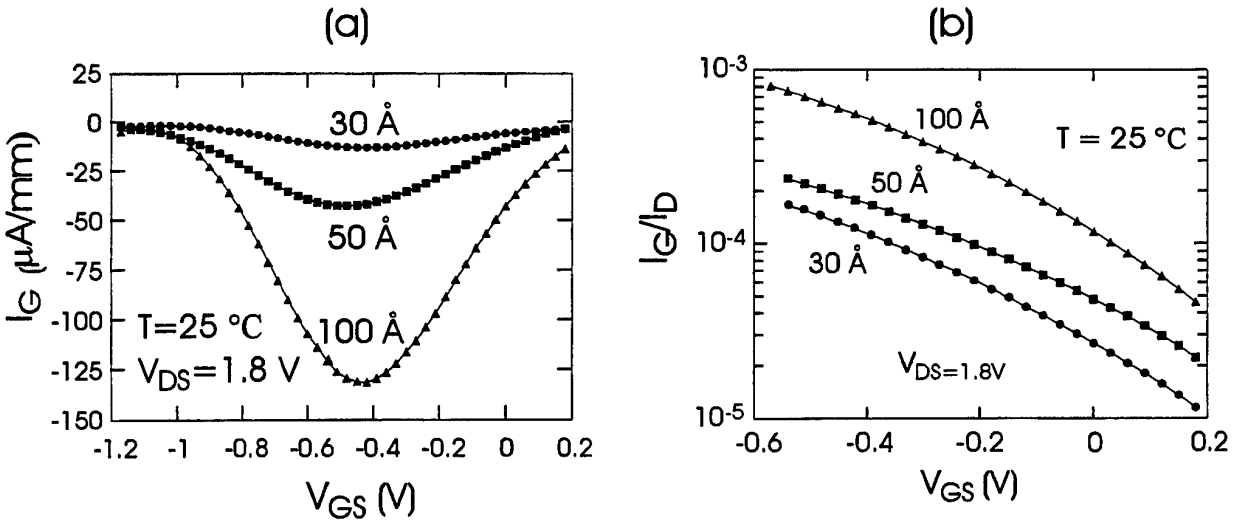

Figure 2.27: I_G vs V_{GS}, measured at V_{DS} = 1.8 V (**a**), and I_G/I_D versus V_{GS}, measured at V_{DS} = 1.8 V (**b**), for composite-channel HEMTs with different $In_{0.53}Ga_{0.47}As$ channel thickness: 30 Å, 50 Å and 100 Å.

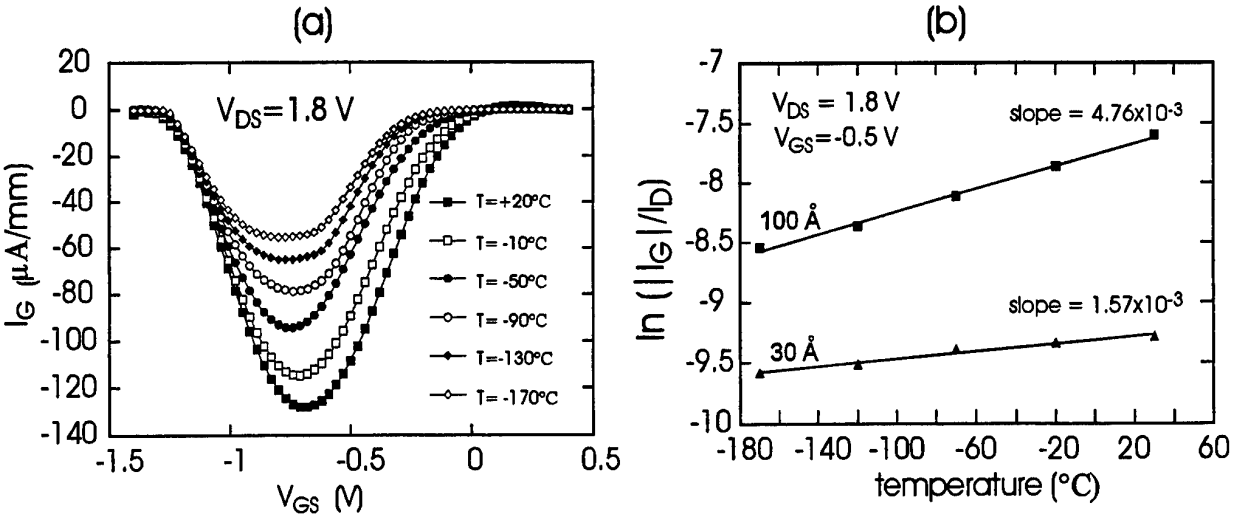

Figure 2.28: (**a**) I_G vs V_{GS}, measured in the device having a 100 Å $In_{0.53}Ga_{0.47}As$ channel thickness at V_{DS}= 1.8 V, for various temperatures. (**b**) $\ln(I_G/ I_D)$ as a function of temperature for composite-channel HEMTs with a $In_{0.53}Ga_{0.47}As$ channel thickness of 30 Å and 100 Å.

We have also carried out measurements of the temperature dependence of the gate current I_G and of the multiplication ratio $| I_G | /I_D$ in the 30 Å and 100 Å channel devices. Figs. 2.28(a) and 2.28(b) shows I_G and $\ln(I_G/ I_D)$, respectively, as a function of temperature over a range of -170°C to 30°C. Differently from all GaAs-based FETs, in our InP-based HEMTs, both I_G and $| I_G | /I_D$ show a positive temperature coefficient, in agreement with the positive coefficient of the electron ionization coefficient α_n in $In_{0.53}Ga_{0.47}As$ shown in Section 1 [11, 15].

2.2.4 Off-State Breakdown Characteristics

Drain-source off-state breakdown voltages have been measured by adopting the drain-current injection technique described in [90]. The breakdown voltage V_{BDS} is unambiguously defined as the maximum drain-source voltage the pinched-off device can attain for a given drain-current density, defined as I_D

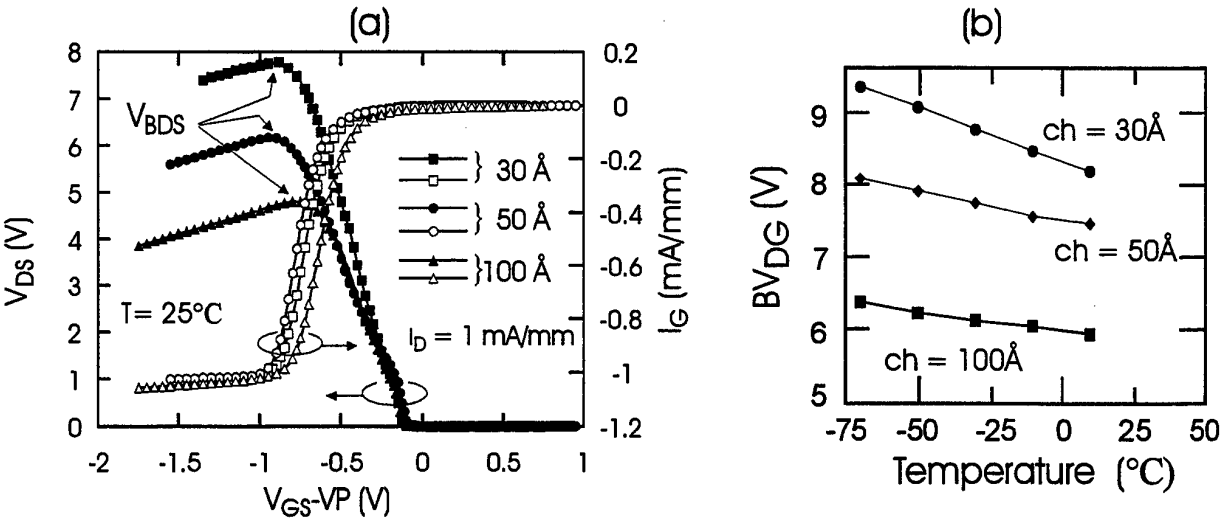

Figure 2.29: **(a)** Drain-source off-state breakdown in composite-channel devices with different channel thicknesses. **(b)** Drain-source off-state breakdown voltage as a function of temperature for composite-channel HEMTs with different channel thickness.

= 1 mA/mm.

Fig. 2.29(a) shows the measured drain-source off-state breakdown in composite-channel devices with different $In_{0.53}Ga_{0.47}As$ channel thickness. The observed V_{BDS} is substantially increased from 4.8 V (100 Å channel) to 6.2V (50 Å channel) to 7.8V (30 Å channel), at I_D = 1 mA/mm. For all devices the off-state breakdown voltage, BV_{DG} decreases with increasing temperature as shown in Fig. 2.29(b).

2.2.5 Discussion

On-State Breakdown

In InAlAs/InGaAs/InP HEMTs the on-state breakdown is dominated by impact ionization in the channel, and its low value is due to the low breakdown field of the $In_{0.53}Ga_{0.47}As$ channel [98]. In composite channel devices, the understanding of breakdown effects is complicated by the presence of a double channel, composed by materials having different energy gaps and, consequently, different ionization energies.

To explain the reduction in ionization rate with decreasing channel thickness one should take into account the influence of (at least) three factors: 1) the changes in the longitudinal electric field in the channel and in I_D consequent to the variations in channel thickness and channel electron concentration; 2) channel quantization effects, and 3) real space transfer of electrons from the InGaAs to the InP layer of the composite channel. We will now discuss the three factors separately.

As can be seen from Table 2.1, a reduction of the InGaAs channel thickness is accompanied by a reduction in the electron sheet density n_s. In order to take into account the corresponding reduction in the drain current, the gate current has been normalized to I_D. As introduced before, the ratio $|I_G|/I_D$ has been demonstrated to be proportional to the value of the electron ionization coefficient α_n in the high electric field region of the channel (under the drain end of the gate), at least as far as ionization events by secondary carriers are negligible [87, 109]. This means that I_D represents the primary electron current initiating impact ionization, while I_G is due to the collection of part of the generated holes at the gate electrode. Due to the nearly exponential dependence of the electron ionization coefficient α_n on the longitudinal electric field in the channel (see Eq. 2.1, the ratio $|I_G|/I_D$, is very sensitive to variations in the electric field. Since the reduction of the electron sheet density, spanning

from $4.2 \cdot 10^{12}/cm^2$ (100 Å channel) to $3.7 \cdot 10^{12}/cm^2$ (30 Å channel), may induce a decrease in the longitudinal electric field, this decrease could contribute to the observed reduction of the $| I_G | / I_D$ ratio.

The effect of channel quantization is to raise the first quantized energy level of conduction electrons in InGaAs and to reduce the conduction band-offset between InGaAs and InP. A contribution to the observed reduction of impact ionization with decreasing channel thickness can be attributed to both effects, that originate from channel quantization. First, if the channel thickness is decreased, the shift of the first quantized energy level results in an enhancement of the effective bandgap energy $E_{G,eff}$ of the $In_{0.53}Ga_{0.47}As$ channel and in an increased threshold energy for impact ionization. Data reported in Fig. 2.25(b) demonstrate this trend, though an accurate calculation of the actual $E_{G,eff}$ shift, as pointed out in section 2.2.2, would require a self-consistent solution of both the Schrödinger and the Poisson equation. Consequently, α_n will be reduced, resulting in a decreased impact ionization current I_G. Second, it is reasonable to assume that the reduced conduction band-offset between InGaAs and InP results in an increased real space transfer of electrons from InGaAs to InP at a certain electric field. To understand how this can lead to a decrease in impact ionization current I_G, we refer to the results reported in [104] regarding the distribution of current in the InGaAs and the InP layers of the composite channel structure: in the low field region near the source, virtually all electrons move in the InGaAs; in the high field region at the drain end of the gate approximately 90% of the electrons are found in the InP subchannel and only a few conduction electrons move in the InGaAs ($\sim$ 10%). A comparison of the α_n data on impact ionization in InP [110] and the data of InGaAs [111], at the same electric field, reveals a difference in ionization coefficient of several orders of magnitude. Therefore, despite in the high electric field region, where impact ionization takes place, 9 out of 10 electrons travel in the InP sub-channel, the contribution to the overall impact ionization generation rate comes mainly from primary electrons moving in the InGaAs channel. In addition, the drain-source voltage is so low in our experiments ($V_{DS} \approx 2$ V) that electrons in InP may not gain enough energy to reach the ionization threshold at all. Even neglecting the above mentioned quantization effect, reducing the InGaAs channel thickness increases the amount of real space transfer to the InP, thus decreasing the fraction of primary electrons able to impact ionize significantly, and, as a consequence, the ionization current I_G. The ratio $| I_G | / I_D$ is still proportional to the ionization coefficient an in InGaAs, but the proportionality factor depends on the channel thickness, due to the fact that only a fraction of the electrons in I_D travel in the InGaAs channel, while those in InP do not impact ionize significantly.

In conclusion, channel quantization effectively reduces impact ionization effects in on-state breakdown due to an enhancement of the channel bandgap (and consequently, an increased threshold energy for impact ionization in InGaAs), due to an increased real space charge transfer from InGaAs to InP, and, possibly, due to a decrease of the longitudinal electric field in the channel.

Measurements of the multiplication coefficients in InGaAs collector HBTs, reported in Section I, have demonstrated that, as opposed to most other semiconductors, the impact ionization coefficient α_n in that material increases with increasing temperature [11, 15]. This anomalous behavior seems to be related to the low density of states near the bottom of the conduction band of $In_{0.53}Ga_{0.47}As$, which could make the ionization process more sensitive to the reduction of the energy gap rather than to the increased phonon scattering, as temperature is raised. Indeed, we observe an increase in I_G and $| I_G | / I_D$ with increasing the temperature in these composite channel devices, as shown in Figs 2.28(a) and 2.28(b). It should be noted, however, that in this case, in addition to the contribution from the positive temperature dependence of α_n, there could be an additional contribution due to the fact that the secondary holes generated in the InGaAs channel must overcome a discontinuity in the valence band, possibly by thermionic emission, to reach the gate electrode and contribute to I_G. This would make the hole collection efficiency of the gate an increasing function of temperature.

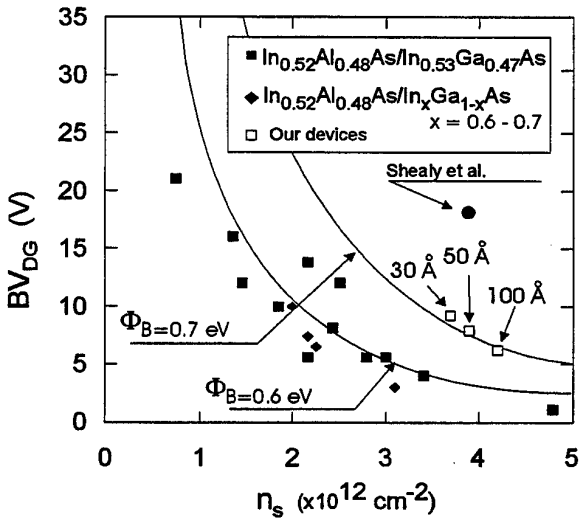

Figure 2.30: Comparison of the off-state breakdown voltage as a function of extrinsic carrier concentration for given gate technologies. From [116] and [121] with modifications.

Off-state breakdown

The off-state breakdown voltage in InAlAs/InGaAs/InP HEMTs is believed to be dependent on a combination of tunneling or thermionic-field emission of electrons from the gate into the channel, and impact ionization in the channel [95]. Electrons are initially injected from the gate edge into the high-field drain-gate region of the insulator by thermionic-field emission. Subsequently, as a consequence of the large electric field in the insulator and the substantial conduction-band offset, they enter the channel hot, and relax their energy through impact ionization.

In the devices tested during this work, the reduction in the InGaAs channel thickness in InAlAs/InGaAs/InP composite HEMTs improves the off-state breakdown voltage through two effects: (i) it reduces the effective electron concentration in the extrinsic gate-drain region, thus decreasing the electric field beneath the gate, which controls the tunnelling current; (ii) it reduces impact-ionization in the channel, due to the enhancement in the effective channel band-gap, already mentioned. Our measurements revealed a substantial increase in BV_{DS} from 4.8 V (100 Å channel) to 6.2 V (50 Å channel) to 7.8 V (30 Å channel), at I_D= 1 mA/mm.

Somerville and del Alamo have developed a model for off-state breakdown of power HEMTs [112], which is based on the assumption that off-state breakdown is largely determined by tunnelling and/or thermionic field emission. In their model, the electric field beneath the gate is calculated by solving a simplified one-dimensional problem, following the treatment originally developed by Frensley [59] for MESFET avalanche breakdown. The electric field is maximum at the gate edge, and its value at this position determines the gate current, which is entirely ascribed to tunnelling [112] or thermionic-field emission over the gate Schottky barrier [113]. Off-state breakdown voltage is determined when this gate current reaches a pre-defined density (normally 1 mA/mm). Differently from [114], the authors in [112, 113] are not interested in determining the onset of gate current instability and irreversible breakdown conditions.

In [112, 113] the authors demonstrate that the most significant variables in determining the off-state breakdown voltage of power HEMTs are the sheet carrier concentration in the extrinsic gate-drain region $n_s(ext)$, and the gate Schottky barrier height, Φ_B. Although it should be mentioned that there is no general agreement on the role of tunnelling current in determining HEMT breakdown [115, 116, 9], (but this is also a result of the very different definitions of off-state breakdown present in the literature), the model in [112, 113] provides an excellent prediction of breakdown voltage dependence on ns, Φ_B,

and temperature, and accurately describes the gate current and its activation energy as a function of V_{DG} [113].

Figure 2.30 shows the predicted off-state breakdown voltage at 1 mA/mm for Φ_B = 0.6 eV and 0.7 eV. Data taken from [112] are compared with data concerning our devices, which adopt a higher Al concentration in the $Al_yIn_{(1-y)}As$ Schottky layer (y=0.60 instead of y=0.48), thus providing a slightly higher Φ_B. As shown in Fig. 2.30, the model accurately predicts off-state breakdown voltage of composite channel HEMTs, defined as the level at which a tunnelling/thermionic-field emission gate current density of 1 mA/mm takes place. Breakdown voltage measurements as a function of temperature are also in agreement with this thermionic/field-emission model; as described in Fig. 9, off-state breakdown voltage decreases as a function of temperature; the absolute reduction being larger for devices having higher n_s(ext) [113].

Figure 2.30 also demonstrates the superiority of this composite channel design with respect to conventional structures; it should be stressed, however, that considerable improvements can be obtained by adopting a composite channel structure having regrown ohmic contacts rather than alloyed ones [117]. Gate-drain (source floating) breakdown voltages up to 18 V have been recently reported for a 50 Å InGaAs 150 Å InP composite channel HEMT with $n_s = 4 \cdot 10^{12} cm^{-2}$.

Part II

Reliability of PMHEMTs and InP HEMTs

Chapter 3

Hot-carrier-induced degradation in pseudomorphic HEMTs on GaAs and in InP-based HEMTs

3.1 Hot-carrier-induced degradation in PM-HEMTs

3.1.1 Introduction

In this section we will present data concerning the degradation mechanisms of PM-HEMT's biased in impact-ionization regime which are crucial for the evaluation of the reliability of power devices. After accelerated testing, a permanent degradation has been found, consisting in the decrease of drain current I_D and of the absolute value of the pinch-off voltage V_p, at low drain-source voltage V_{DS}, resulting in the development of a remarkable "kink" in the output characteristics. DC, pulsed and low-frequency AC measurements demonstrate that the failure mechanism consists in the creation of deep levels under the gate which act as electron traps at low gate-to-drain electric fields. Deep Level Transient Spectroscopy (DLTS) and photoinjection measurements reveal the presence of two levels at 0.77 eV and 1.22 eV. The intensity of the 1.22 eV peak is correlated with the degradation observed in stressed devices.

3.1.2 Hot-electron degradation

Packaged PM-HEMTs devices of the same type described in paragraph 2.1.3 and depicted in Fig. 2.6(a) were submitted to various accelerated tests, including: (a) pure thermal storage tests with no applied bias at temperatures ranging from 150°C to 300 °C; (b) long-term (up to 10^4 minutes) hot-electron tests at room temperature, at various drain-to-source, V_{DS}, and gate-to-source, V_{GS}, biases. The latter tests were carried out at high V_{DS} values (from 6 to 8 V), in a remarkable impact-ionization regime, testified by the presence of a non-negligible negative gate current I_G and of light emission, as shown in Fig. 2.6(b).

No decrease in the saturation drain current I_D, or change in the pinch-off voltage V_p was found during thermal storage tests.

On the contrary after hot-electron tests we observed a failure mode consisting of a noticeable decrease of the drain current, I_D, occurring at low V_{DS} bias, $V_{DS} \leq 2$V. Figure 3.1(a) shows the output characteristics of a W = 180 μm device before and after 137 hours of hot-carrier stress test at V_{DS} = 7.5 V, V_{GS} = - 0.1 V. The thermal resistance of packaged devices was measured as $\simeq$ 100 °C/W. Since hot electron tests have been carried out at room temperature with a dissipated power of about 0.4 W, the real junction temperature during these tests was estimated as being $\simeq$ 65 °C.

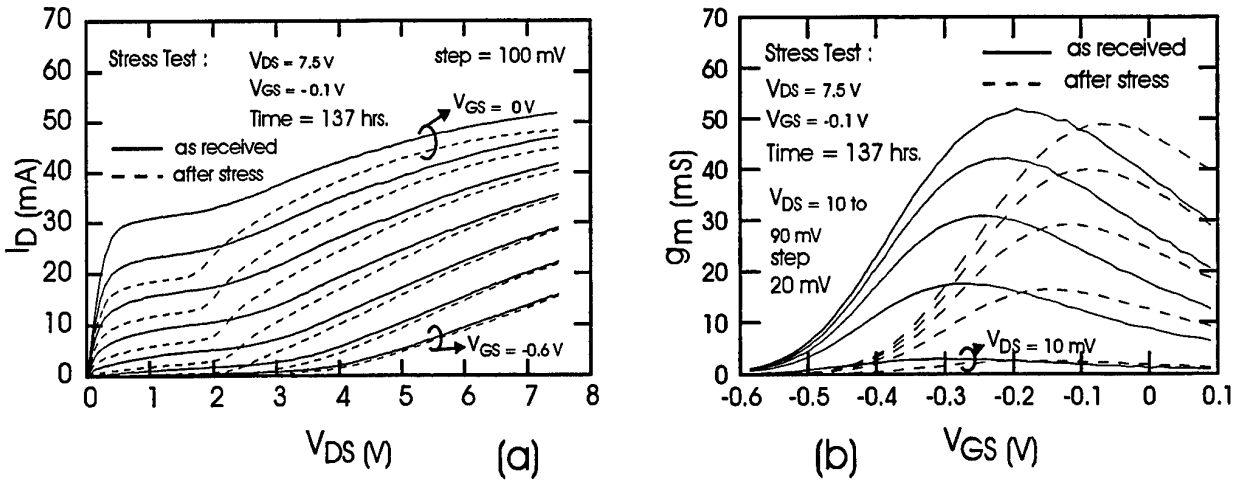

Figure 3.1: **(a)** Device output characteristics before (continuous line) and after (dashed line) 137 hrs of hot electron stress test at V_{DS} = 7.5 V, V_{GS} = -0.1 V. The noticeable increase of the "kink" in the I_D is clearly visible at low V_{DS}, V_{DS} < 2 V, in the stressed device. **(b)** $g_m(V_{GS})$ measured before (continuous line) and after (dashed line) 137 hrs of hot electron stress test at V_{DS} = 7.5 V, V_{GS} = -0.1 V.

A "kink" in the I-V curves can be observed in the unstressed device at $V_{DS} \simeq 2$ V. After the hot electron accelerated test, the amplitude of this "kink" is remarkably enlarged, at low drain voltages, $V_{DS} \leq 2$ V, owing to the decrease of I_D, dashed lines in Fig. 3.1(a). The degradation is permanent, and can not be recovered by annealing the stressed devices up to 250 °C, 24 hours.

By plotting the transconductance measured in the linear region, Fig. 3.1(b), we can notice that the degradation induced in the low V_{DS} region of I-V characteristics mostly consists in a decrease of the absolute value of the pinch-off voltage, $|\Delta V_p| \simeq 130$ mV. This shift is consistent with an increase in the negative charge trapped under the gate.

No degradation has been observed of source or drain parasitic end-resistances measured with the Lee-Shur method, [118], indicating that the damage takes place mainly in the gate region of the device, as suggested by the occurrence of the $|V_p|$ shift.

The rate of degradation increases nearly exponentially with V_{DS}, see Fig. 3.2(a) and (b); i.e. the degradation increases at increasing the number of high energy electrons. On the other hand, the degradation is very sensitive also to V_{GS}, i.e. the degradation is less severe when devices are biased near the pinch-off region and only few hot-electrons are available in the channel.

3.1.3 Deep level characterization

The above described experimental data suggest that hot electron accelerated tests induce, in stressed devices, an increase in the density of deep electron traps under the gate. When negatively charged, these traps can cause the shift in the pinch-off voltage and the decrease in I_D previously described.

To verify this hypothesis, we carried out an extensive characterization of traps present in stressed samples as well as in untreated ones, by means of transconductance frequency dispersion, optical and DLTS analyses.

As well known, deep traps can give rise to several anomalies of HEMT transistors. Kink effects [119], low-frequency transients [120] and changes of the transconductance as a function of frequency, [120, 121, 122], are typical indicators of the presence of traps in HEMT devices. In particular deep levels present in the gate-drain and gate-source access regions induce a decrease in $g_m(f)$ on increasing the frequency [121], while deep levels, such as the DX centers, present under the gate are responsible

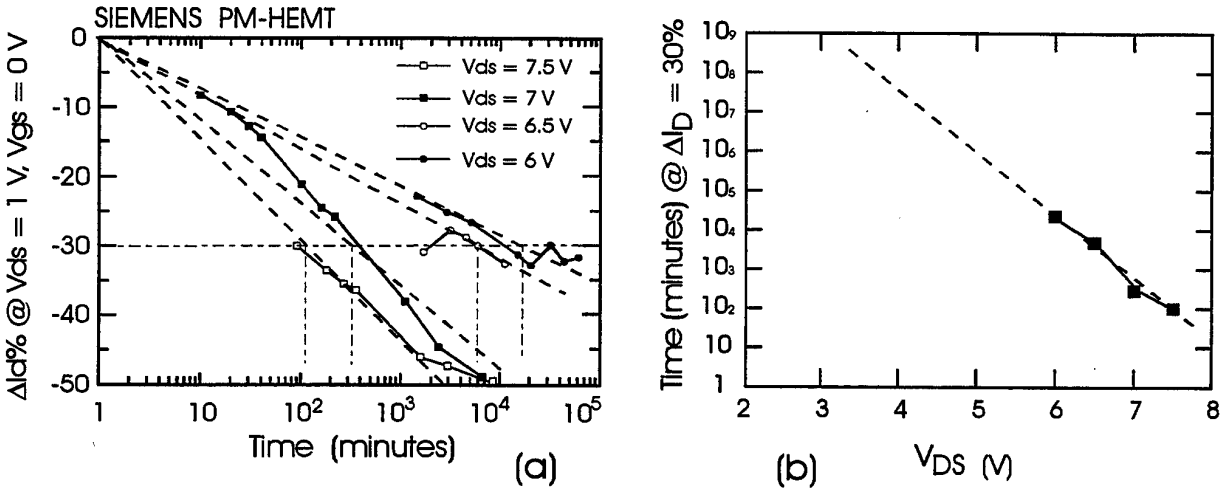

Figure 3.2: **(a)** I_D degradation measured at $V_{DS} = 1$ V, $V_{GS} = 0$ V during the hot-electron stress test for different V_{DS} values during the stress. **(b)** Time to reach the 30 % I_D degradation as a function of the V_{DS} applied during the hot-electron stress test.

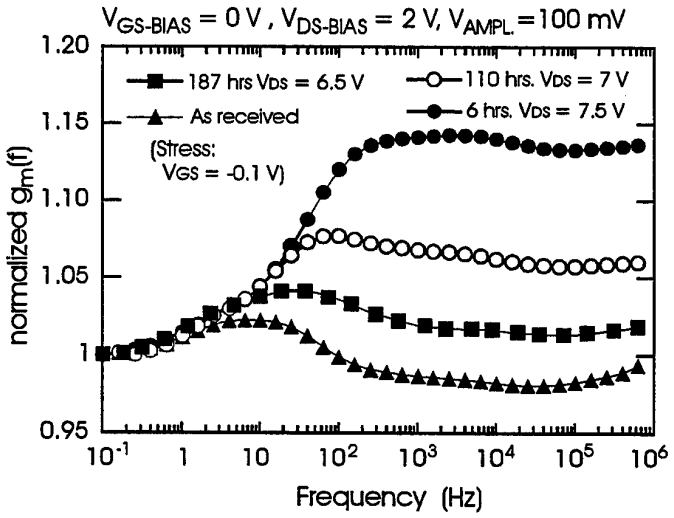

Figure 3.3: Normalized transconductance frequency dispersion $g_m(f)$ measured at room temperature in devices after different hot electron stress tests. On increasing the V_{DS} voltage during hot electron stress test the $g_m(f)$ dispersion increases.

for an upward dispersion of $g_m(f)$ [122, 123]. At low frequency, the device transconductance is affected by the modulation of the charge trapped on deep levels. On increasing the frequency, traps can no longer follow the signal applied to the gate thus causing the change in the normalized transconductance. In particular $g_m(f)$ starts to change when the signal period becomes comparable with the characteristics trap times and reaches its maximum change when the signal period becomes shorter than capture/emission time [121, 122, 123].

Figure 3.3 shows the transconductance as a function of frequency in the $10^{-1} \div 10^6$ Hz frequency range measured at room temperature on devices submitted to different hot-electron tests. For $g_m(f)$ measurements the devices have been biased at $V_{DS-BIAS} = 2$ V, $V_{GS-BIAS} = 0$ V. The $g_m(f)$ have been evaluated applying a 200 mV peak-to-peak amplitude sinusoidal signal at the gate, V_{AMPL}, at

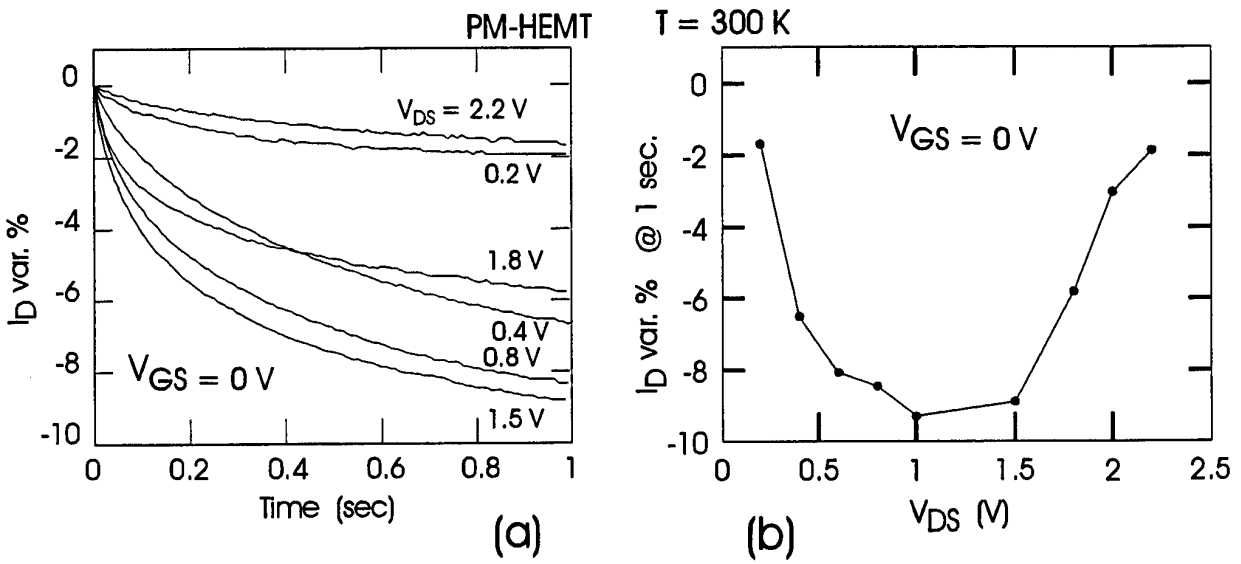

Figure 3.4: **(a)** Drain current transients observed at room temperature in a PM-HEMT's after hot electron stress test (V_{DS} = 7.5 V V_{GS} = - 0.1 V, 137 hrs.). Keeping V_{GS} = 0 V pulses of various amplitude (0.2 V $\div$ 2.2 V) and duration up to 10 ms are applied to the drain. **(b)** Percent decrease of I_D measured after 1 s during transient.

different frequencies. For each device, the normalized transconductance at a certain frequency f is defined as $g_m(f)$ / $g_m(0.1\ Hz)$, where $g_m(0.1\ Hz)$ is the transconductance evaluated at 0.1 Hz.

Untreated devices show a slight decrease in transconductance at high frequencies, possibly due to the presence of deep levels in the drain/source access regions. On the contrary, transconductance remarkably increases as a function of frequency in devices after hot electron test, thus indicating generation of traps under the gate.

Higher trap density corresponds to a larger transconductance frequency dispersion. On increasing the V_{DS} applied during the hot electron test, and the consequent degradation of I_D, an increased dispersion of the transconductance is measured, which may be explained by the increase in the density of deep levels under the gate and the enhancement of electron trapping with the consequent increase of the negative charge accumulated under the gate.

Electron trapping can be directly observed during transient measurements on devices which suffered parametric degradation after hot-electron tests. Keeping V_{GS} at 0 V, we applied drain voltage pulses of various amplitudes (0.2 V $\div$ 2.2 V) and very long duration (up to 10 s). During the transients the drain current, I_D decreases as a consequence of the electron trapping and of the increase in the negative charge accumulated under the gate. The I_D transient times are very long (hundreds of milliseconds), see Fig. 3.4, consistent with the low frequency at which the $g_m(f)$ dispersion occurs. This correlation confirms that the increase of the transconductance frequency dispersion in devices submitted to hot-electron stress test is due to trapping of electrons and occurs when trapping time become larger than the sinusoidal signal period. The total I_D variation observed after 1 s of biasing at different V_{DS} is plotted in Fig.11 b). As it can be seen, the degradation of I_D first increases on increasing V_{DS}, then shows a maximum at a V_{DS} value of $\simeq$ 1.5 V (corresponding to the V_{DS} value at which the kink occurs); while for larger V_{DS} values the I_D variation steeply decreases on increasing V_{DS}. In the as received devices a similar behaviour has been observed but the drain transient degradation is not as prominent as in the degraded devices.

Another way of characterizing trapping effects is to look at the behaviour of devices under illumination [124, 125]. As it could be expected, photoionization of electron traps induces a recovery of the

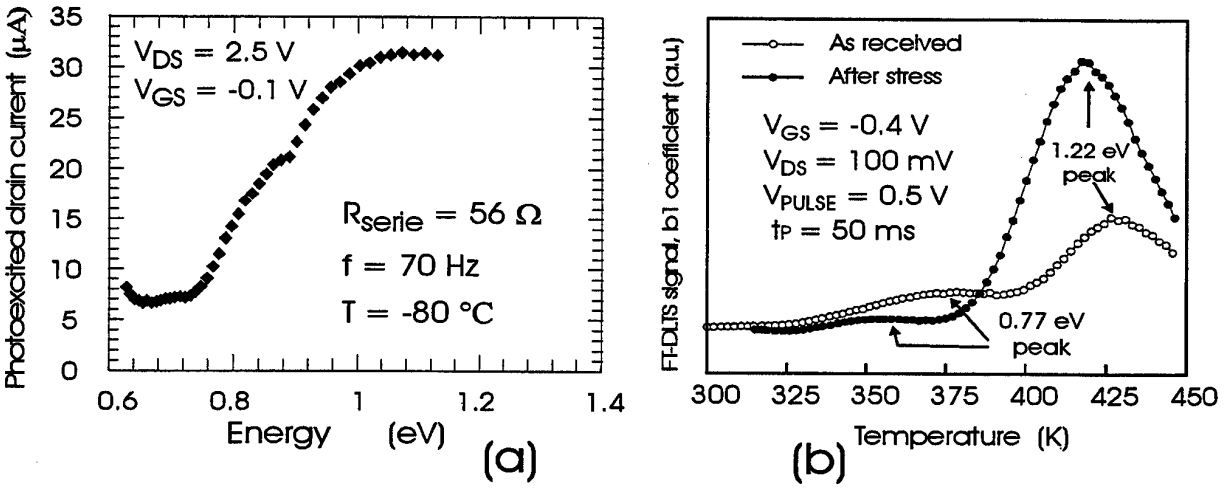

Figure 3.5: **(a)** Photoexcited drain current measured using a lock-in technique as a function of the energy of exciting photons in in a stressed device (V_{DS} = 7.5 V, V_{GS} = -0.1 V, 137 hrs). **(b)** Drain Current FT-DLTS measurements in an as received device (open simbols) and in a device after hot electron stress test: V_{DS} = 7.5 V, V_{GS} = - 0.1 V, 137 hrs (closed simbols).

output characteristics of degraded devices and completely eliminates the "kink" effect, thus confirming the origin of the observed degradation. In order to better understand the nature of the generated deep levels, we adopted the photocurrent measurement technique described in [126]. The biased sample is illuminated with chopped monochromatic light in the 0.6 eV ÷ 1.1 eV energy range. Energy of illuminating photons was limited to 1.1 eV to avoid direct band-to-band electron-hole generation in the $In_{0.2}Ga_{0.8}As$ channel. The variation of I_D was measured using a lock-in technique. A sharp step in I_D indicates a change of the charge state of the corresponding trap level [124]. Two of these sharp transitions are clearly observed in Fig.3.5(a): one at $\simeq$ 0.74 eV and the other one at $\simeq$ 0.89 eV.

Finally, drain current DLTS (Deep Level Transient Spectroscopy) spectra have been adopted to identify deep levels. Measurements were performed using Fourier-Transform DLTS (FT-DLTS) [127]. In FT-DLTS, the discrete Fourier coefficients are calculated at each temperature by a numerical Fourier transformation of a complete transient. The resulting Fourier coefficient spectra versus temperature contain information about the trap levels and allow one to obtain capture cross-section and activation energies of the levels. The first cosine coefficient spectrum has been considered, since it represents a good trade between a high signal-to-noise ratio and a high emission rate resolution. The samples were biased as the following: source grounded, V_{DS} = 100 mV and V_{GS} = -0.4 V. The gate was pulsed at V_{PULSE} = 0.5 V for t_p = 50 ms.

Current DLTS spectra of untreated devices reveal two peaks, corresponding to two electrons traps with an activation energy of Ea = 0.77 eV and Ea = 1.22 eV respectively, see Fig.3.5(b). These traps have been already observed by P. M. Mooney et al. [128] in MBE-grown AlGaAs. Hot electron testing induced a remarkable increase in the intensity of the 1.22 eV peak, see Fig.3.5(b), thus suggesting a corresponding increase in the electron trap density. The shift towards low temperature of the peaks in the stressed samples may be caused by the decrease of the absolute value of the pinch-off voltage induced by the hot-electron stress above reported.

As last results, gate diode electrical characteristics have also been investigated. Negligible degradations have been observed in both forward ideality factor and Schottky barrier height, as well as in reverse breakdown voltage. Furthermore, an increase of the generation-recombination forward current has been observed after the hot-electron stress in stressed devices.

3.1.4 Discussion

We have also reported on a new, permanent degradation mechanism induced by hot electron in GaAs based power PM-HEMT's. Both gate current and electroluminescence measurements demonstrate that significant hot-electron effects (impact-ionization and light emission) take place in the pseudomorphic AlGaAs/InGaAs HEMT's under test when operated at drain voltage above 5 V. Untreated devices appear to be affected by the presence of deep levels, testified by the presence of a slight "kink" effect in the output characteristics [119, 125], see Fig. 2.6(b) and Fig. 3.1(a), and by the observation of two peaks at 0.77 eV and 1.22 eV in the DLTS spectra, see Fig. 3.5(b).

Significant degradation of the output characteristics takes place when devices are operated in hot electron regime at $V_{DS} \geq 6$ V. In particular, the amplitude of the kink in the output characteristics increases, corresponding to an increase of the device pinch-off voltage, $\Delta|V_P| \simeq 130$ mV, and a corresponding decrease of I_D occurring at low V_{DS}, see Figs. 3.1(a) and (b). The observed degradation is most likely due to an increase in the deep level density in the AlGaAs layer under the gate of the device generated by hot electrons stress [119, 125].

At low V_{DS}, the increased negative charge due to trapped electrons in the AlGaAs layer under the gate causes a large decrease in I_D and the observed shift in the threshold voltage. At high V_{DS}, three effects can contribute to de-trap or compensate the trapped electrons: (i) hot electrons can impact-ionize traps, thus releasing the trapped negative charge [129]; (ii) the high electric field existing between gate and drain can enhance the electrons detrapping; (iii) holes, generated by impact-ionization, can compensate trapped electrons. In all cases, the result is a sudden modulation of the negative charge trapped under the gate and a consequent increase in the drain current, with the creation of a "kink" in the output characteristics [119, 125].

Experimental data also suggest that traps are not created in the source/drain access regions of the device, but rather only under the gate. In fact, no increase in the source and drain end-resistances was observed.

Evidence of an increase in deep level density in failed devices is provided also by pulsed measurements and by low-frequency dispersion ac transconductance measurements, see Fig. 3.3. During pulse measurements, very slow transients in I_D are observed, which correspond to electron trapping phenomena from the channel into the AlGaAs layer. The behaviour of the drain current decrease, ΔI_D, during the transients as a function of the applied V_{DS}, Figs. 3.4(a) and (b), is consistent with the presence of the "kink" in the output I-V V_{GS} DC characteristics. Since electrons must have a non-negligible energy in order to surmount the AlGaAs/InGaAs barrier and be trapped, the amount of I_D degradation initially increases with V_{DS}. For $V_{DS} > 1.5$ V (at $V_{GS} = 0$ V), however, other mechanisms are triggered (such as compensation of trapped electrons with holes generated by impact-ionization, high-field-assisted electron detrapping and impact-ionization of trapped electrons by hot-electrons) which tend to decrease the net trapped negative charge and consequently reduce the I_D degradation. Transient times are extremely slow, with time constants in the 1 ms $\div$ 100 ms range, consistently with the results of $g_m(f)$ measurements.

The identification of the deep levels present in the devices has been carried out by means of photocurrent measurements and of Fourier-transform DLTS. Two levels at 0.77 eV and 1.22 eV have been identified, see Figs. 3.5(a) and (b). In particular, a remarkable increase in the intensity of the 1.22 eV peak, already reported as an electron trap present in MBE-grown AlGaAs layers [128], is observed in devices submitted to hot-electron tests. These very high value of energy is consistent with the very slow trapping/detrapping phenomena observed. Moreover the DLTS measurements confirm the presence of traps in the as received devices and the increase in the trap density induced by the hot electron stress test. This explains: i) the presence, in the as received devices, of "kinks" in the I-V characteristics; ii) the I_D degradation during pulse measurements (not shown); and iii) the increase

of both "kink" amplitude and I_D degradation after hot-electron stress, due to the increase in the trap density.

In conclusion, devices submitted to long-term hot-carrier tests present a new permanent failure mechanism consisting in the creation of deep levels in the AlGaAs layers or at their interfaces in the gate region. These deep levels cause trapping of electrons i.e. accumulation of negative charge under the gate, which gives rise to: i) a correlated decrease of I_D and of the absolute value of pinch-off voltage; ii) a consequent increase of the kink effect; iii) the occurence of anomalies with slow time constants in the device response measured as I_D transients and transconductance frequency dispersion. The density of a deep electron trap at 1.22 eV, identified by means of DLTS measurements, has been observed to remarkably increase after hot electron tests and has been considered as the main responsible for device degradation. The kink in I-V characteristics, which is remarkably enhanced by hot electron stress, appears to be due, in these devices, to a combination of impact ionization and deep-levels, as reported in [125]. Further work is needed in order to identify the physical origin of these traps, and the physical mechanism of generation of deep levels during hot-carrier testing and their location. Finally, it should be stressed that kink effects and degradation phenomena can be reduced by optimizing dry etching conditions of the gate recess and MBE growth temperature.

3.2 Kink and Hot-electron degradation in $In_{0.53}Ga_{0.47}As$/InP HEMTs

3.2.1 Introduction

High performance InAlAs/InGaAs/InP high electron mobility transistors (HEMTs) (with g_m values over 1000 mS $\cdot mm^{-1}$) are characterized by a very thin InAlAs layer (200 Å). A very high sensitivity of the threshold voltage, V_{th}, on the InAlAs thickness is hence present. Moreover, these devices are often affected by kink effects and premature breakdown, both related with the narrow bandgap of the $In_{0.53}Ga_{0.47}As$ channel layer.

It has been recently demonstrated [130] that using an InP-recess-etch stopper, uniformity in V_{th} can be improved thanks to the tight control on the InAlAs layer thickness. We will demonstrate here that the InP-recess-etch stopper layer can passivate the InAlAs in the access regions adjacent to the gate thus eliminating kink effects and improving the long-term stability of the devices when submitted to hot-electron stress tests.

3.2.2 Kink elimination

In this section we report on the elimination of the kink effect in InP-based HEMT's which results from the insertion of an InP etch stop layer.

Kink phenomena represent one of the major problems in the degradation of the electrical characteristics of InP-based HEMT's [100]. In the literature the "kink" effect is usually attributed to: (i) pile-up of holes generated by impact-ionization at the source side [99]; (ii) deep levels in the substrate/buffer or surface layers [125]; (iii) a combination of impact ionization and deep levels [100].

Two InAlAs/InGaAs HEMT's technologies have been studied, with and without InP recess-etch stopper layer. Devices without InP recess-etch stopper are affected by a "kink" in the output I-V characteristics. Despite the similarity of the device structures, and the fact that impact ionization is present in devices, no kink is present in the devices adopting the InP recess-etch stopper layer. Presence of surface traps has been demonstrated by means of transconductance frequency dispersion [121], $g_m(f)$ measurements in devices without the InP stopper, while no $g_m(f)$ dispersion was observed in devices with the InP stopper. The two kinds of devices were also submitted to hot-electron stress test (both in open and close channel condition). The devices DC characteristics initially improve (I_D increases) in all stressed devices. After this 'burn-in'phase, however, we observed a large degradation of both DC and $g_m(f)$ characteristics only in the devices without the InP etch-stopper. We therefore conclude that: a) the InP recess-etch stopper layer effectively removes the kink by passivating the InAlAs surface in the recess regions adjacent to the gate; that b) at least in these structures impact-ionization alone is not sufficient to induce a kink [100]; c) passivation by InP is also effective in reducing hot-electron surface damage, thus improving the reliability of devices operating at high V_{DS}.

3.2.3 Devices and Experimental Results

Figure 3.6 shows a schematic cross section of the 0.1 μm gate length and 10 μm gate width InP-based LM (lattice-matched) HEMTs used in this work [130]. The epitaxial structure grown by MOCVD consists of a 2000 Å thick InAlAs buffer, a 150 Å thick InGaAs channel, a 30 Å InAlAs spacer, a Si-δ-doped plane, a 60 Å InAlAs Schottky barrier, a 50 Å InP-recess-etch stopper (this layer was present in one type of devices and not present in the other one), and n^+-InAlAs/n^+-InGaAs cap layers. We also studied MBE grown InP-based LM (lattice-matched) HEMTs having the same structure except for the following: a) a uniformly doped InAlAs (10^{19} cm^{-3}) donor layer is adopted and b) the InP-recess-etch stopper is not present. In both devices the whole structure is covered by a SiO_2/SiN bi-layer. All materials are lattice matched to the InP substrate.

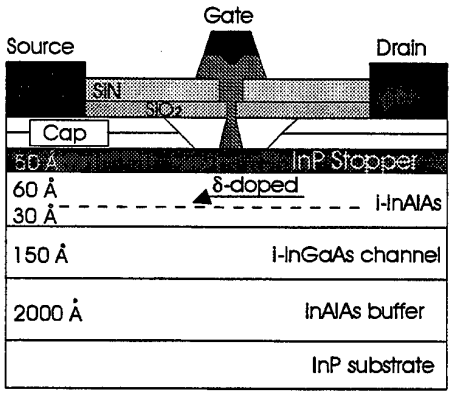

Figure 3.6: Schematic cross section of the InP-based Lattice Matched HEMT.

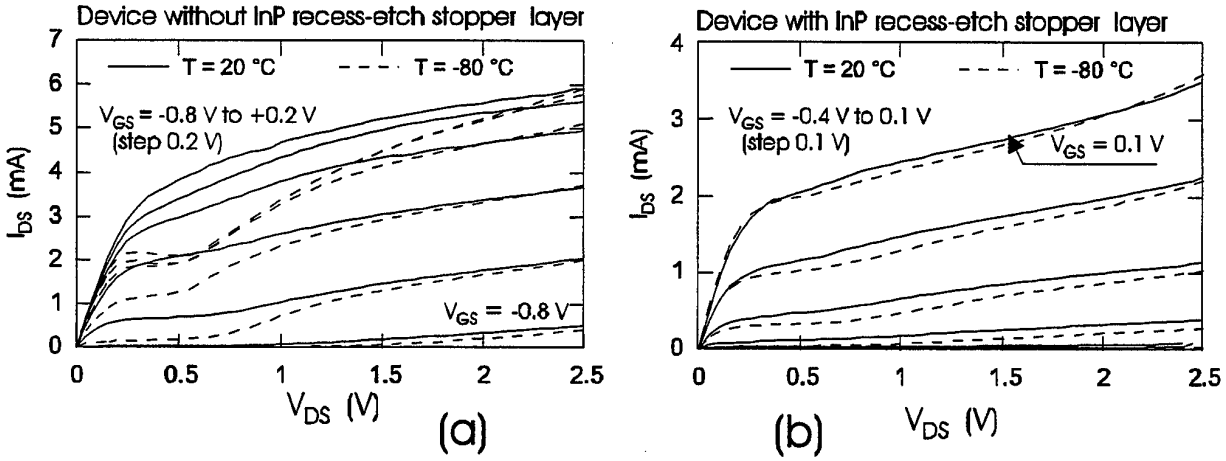

Figure 3.7: I_D vs V_{DS} at different V_{GS} measured at + 20 °C and - 80 °C in a device without InP recess etch stopper **(a)** and in a device with the InP etch stopper **(b)** .

Figure 3.7(a) shows the output characteristics of a typical device without InP recess-etch stopper, carried out at room (+20 °C continuous line) and low (-80°C dotted line) temperature. A considerable collapse of the drain current (at low V_{DS} values) is observed at low temperature due to trapping mechanisms. At higher V_{DS} values the I_D current completely recovers, giving rise to a remarkable kink effect.

Figure 3.7(b) shows the output characteristics of a typical device with InP recess-etch stopper layer at the same temperature values. A negligible decrease in the drain current (in the whole V_{DS} range) is observed at low temperature without any worsening of the kink phenomena. In Fig.3.8(a) the gate current, I_G vs V_{GS} characteristic is shown for different V_{DS} values (V_{DS} from 1.5 V to 2.3V) measured at room (+20 °C continuous line) and low (- 80 °C dotted line) temperature in a device without InP recess-etch stopper. The non monotonic behavior typical of impact ionization, [108] is observed at low temperature thanks to a remarkable decrease in the leakage current. Similar results have been obtained in devices with InP etch stopper layer, see Fig. 3.8(b).

In Fig.3.9(a) the $g_m(f)$ is reported as a function of the gate voltage for V_{DS} = 100 mV in a typical device without InP recess-etch stopper. Noticeable transconductance frequency dispersion is observed. Negative dispersion has been associated to surface states in the access regions and has found to increase at decreasing the gate voltage since surface states are feed by gate leakage current [131]. Figure 3.9(b)

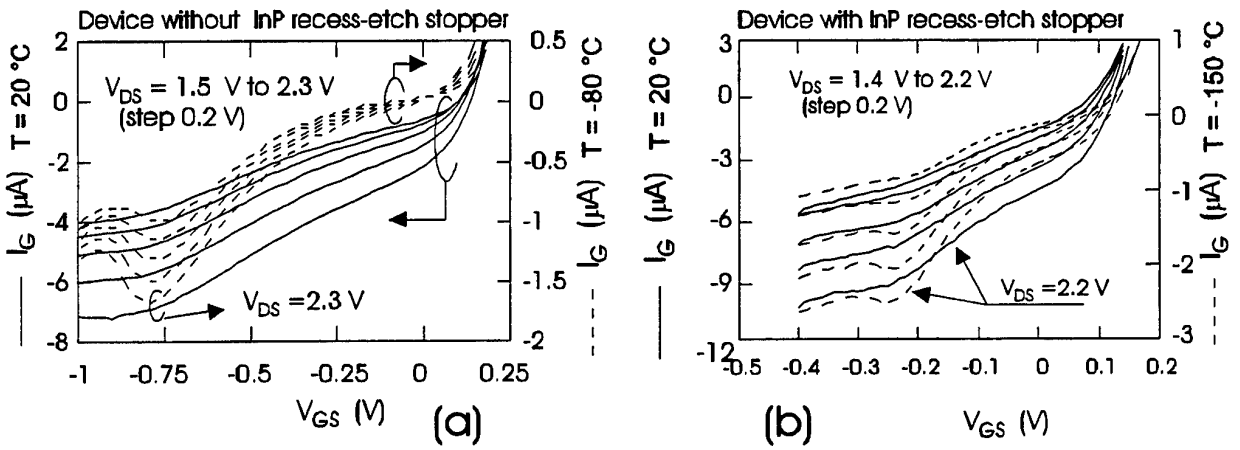

Figure 3.8: I_G vs V_{GS} at different V_{DS} measured at + 20 °C and - 80 °C in a device without InP recess etch stopper **(a)** and in a device with the InP etch stopper **(b)** .

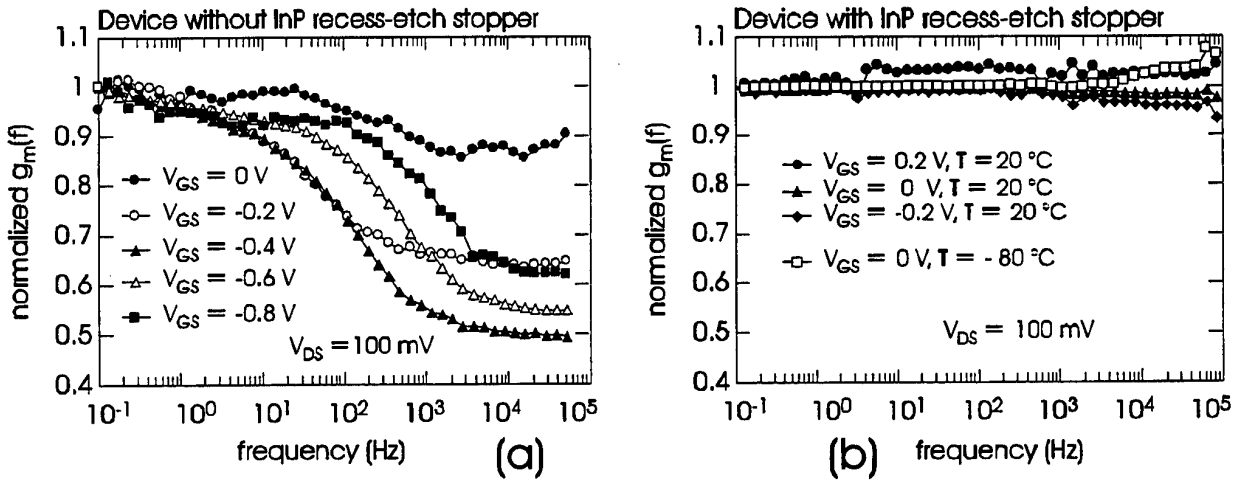

Figure 3.9: **(a)** g_m(f) measured at different V_{GS} (at + 20 °C) in a device without InP recess-etch stopper. **(b)** g_m(f) measured at different V_{GS} (at + 20 °C) and at V_{GS}= 0 V, T = +80 °C in a device with InP recess-etch stopper.

reports the transconductance frequency measurements as a function of the gate voltage for V_{DS} = 100 mV in a typical device with InP stop etch layer. No transconductance frequency dispersion is observed in the whole V_{GS} range. The chosen bias points are different due to the different value of V_{th} in the two devices. In Fig. 3.10 the transconductance frequency dispersion is reported as a function of temperature for V_{DS} = 100 mV and V_{GS} = -600 mV in a device without InP etch stop layer. A shift towards lower frequency is observed on the g_m(f) dispersion on decreasing the temperature. The characteristic frequency f_M is the frequency where the dispersion is half of the total one. By plotting $f_M(T)/T^2$as a function of 1/kT in an Arrhenius plot, a straight line is obtained; see inset of Fig. 3.10. From the slope of this line, an activation energy of 0.28 eV ± 10% has been obtained [132]. No transconductance frequency dispersion is observed at low temperature in devices with the InP stop etch layer, see Fig. 3.9(b).

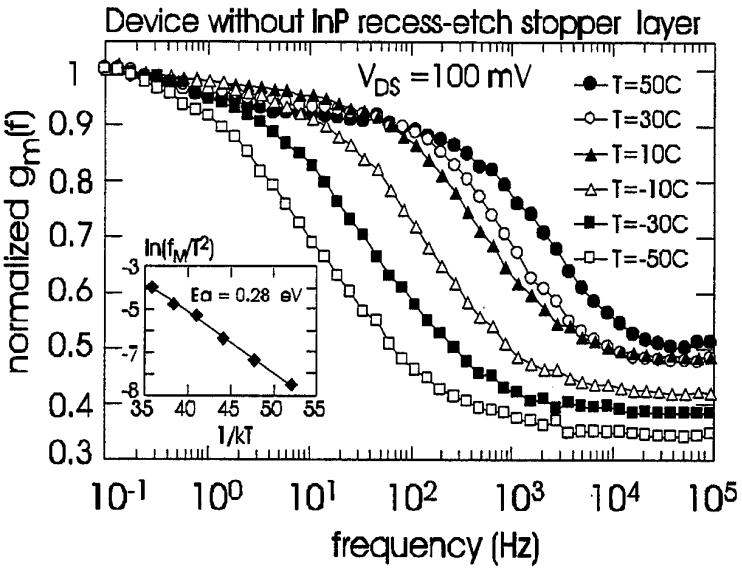

Figure 3.10: $g_m(f)$ measured at different temperatures (V_{DS} = 100 mV, V_{GS}=-0.6 V, in a device without the InP recess-etch stopper. The Ea calculation is depicted in the inset.

3.2.4 Discussion

Kruppa and Boos [131] have associated decrease of transconductance as a function of frequency with surface traps in the gate recess region. They have identified traps with an activation energy of 0.17 eV in the MBE-grown InAlAs/InGaAs/InP HEMTs only in the presence of a double-recess structure. B. Georgescu et al. [133] have recently described kink effects in composite InAlAs/InGaAs/InP composite channel HEMTs, mainly related to trapping/detrapping process in the top layers. The correlation between surface traps and kink in the output characteristics has been demonstrated also by T. Suemitsu et al. [100] by means of two dimensional device simulation. The increased source resistance due to the presence of traps in the gate-to-source access region can be completely compensated by hole pile-up in the channel at the source side due to holes generated by impact-ionization. The pile up leads to an increase of I_D and hence to the appearing of the kink. H. Wang et al. [134] have found that the kink in InAlAs/InGaAs HFETs can be suppressed by using suitable-deposited silicon nitride passivation. Finally R. Menozzi et al. [135] have found a dependence of the hot-electron degradation of InAlAs/InGaAs/InP HEMTs on the presence of PECVD SiN passivation. All these results points to a crucial role of device top layers, especially in the exposed gate recess region, in determining kink effects and low frequency anomalies.

We have studied InAlAs/InGaAs HEMT devices with and without InP recess-etch stopper layer which passivates the gate recess regions. Devices without InP recess-etch stopper are affected by a kink in the output I-V characteristics, which is enhanced at low temperature, see Fig. 3.7(a). On the contrary kink effect is not observed in the devices with InP etch stop layer even at low temperature, see Fig. 3.7(b). Transconductance frequency dispersion have been observed in devices having a free InAlAs surface, see Fig.3.9(a), while no $g_m(f)$ dispersion was observed in devices with the InP stopper, see Fig.3.9(b). Our measurements demonstrate that devices without the InP stop etch layer are affected by surface states, having Ea = 0.28 eV, see Fig. 3.10, in the gate-drain and gate-source access regions while devices with the InP etch-stopper do not show any evidence of surface state presence; I_G measurements demonstrate that impact ionization is present in both devices (see Figs. 3.8(a) and 3.8(b)).

Following these experimental results we have demonstrated that traps in the gate-source and gate-

drain access region are present in devices without InP etch stopper layer. These traps can become negatively charged due to capture of electrons leading to a reduction of I_D at low V_{DS}. On increasing V_{DS} the modification of potential profile in the source-gate recess region caused by the compensation of the negative trapped charge by holes generated by impact ionization and/or field assisted electron detrapping leads to a recovery of the drain current thus originating the kink effect [100]. Devices adopting the InP etch stopper layer are free from surface traps, and therefore are not affected by kinks even in the presence of impact ionization.

3.2.5 Hot-electron degradation

Devices have also been submitted to hot electron stress test with the following results:
a) *devices without the InP etch-stopper*: A first test has been carried out at V_{DS} = 3 V, V_{GS} = -0.8 V, (corresponding the peak in the I_G current, see Fig. 3.8(a), and hence to the highest impact-ionization). An increase in I_D is initially observed (for t $\leq$ 1 hour), see Fig. 3.11(a); subsequently, a large degradation of I_D is observed, and a large kink in the output characteristics is developed, Fig. 3.11(b).

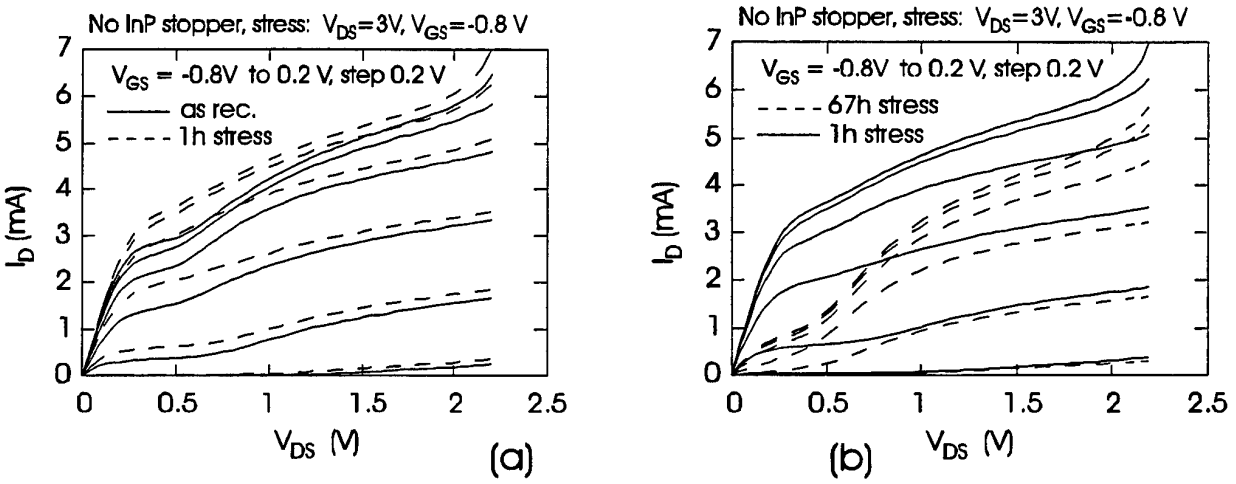

Figure 3.11: **(a)** I_D vs V_{DS} at different V_{GS} measured before and after 1 hr of stress at V_{DS} = 3V, V_{GS} = -0.8 V, in a device without the InP etch-stopper. **(b)** I_D vs V_{DS} at different V_{GS} measured after 1 hr and after 67 hrs of stress at V_{DS} = 3 V, V_{GS} = -0.8 V in a device without the InP etch-stopper.

Development of surface states takes place mostly in the gate-drain region, so that degradation is enhanced if source and drain are swapped during measurements, see Fig. 11. Moreover, the degradation is accompanied by an increase in downward transconductance frequency dispersion, see Fig. 12, which confirms the development of additional surface states in the access regions. A similar two-steps degradation behavior, but with slower changes, is observed when the devices are biased close to pinch-off (V_{DS} = 3 V, V_{GS} = -1 V) and by biasing the devices in gate-to-drain breakdown conditions ($I_G = -10\mu$A, V_{GD} =-6 V), i.e. with a high electric field and impact-ionization, but with very reduced primary electron current and power dissipation. The degradation observed after 20 hours of stress in breakdown conditions (second step) is shown in Fig. 13.
b) *devices with the InP etch-stopper* Devices were tested at various bias points, corresponding to approximately the same gate current or dissipated power measured during the tests of HEMTs without InP etch stopper. The only observed variation is an increase in I_D similar to the one observed in the initial phase of testing of devices without the InP stopper. The I_D increase is correlated to a corresponding increase in the absolute value of the device pinch-off voltage, possibly related to

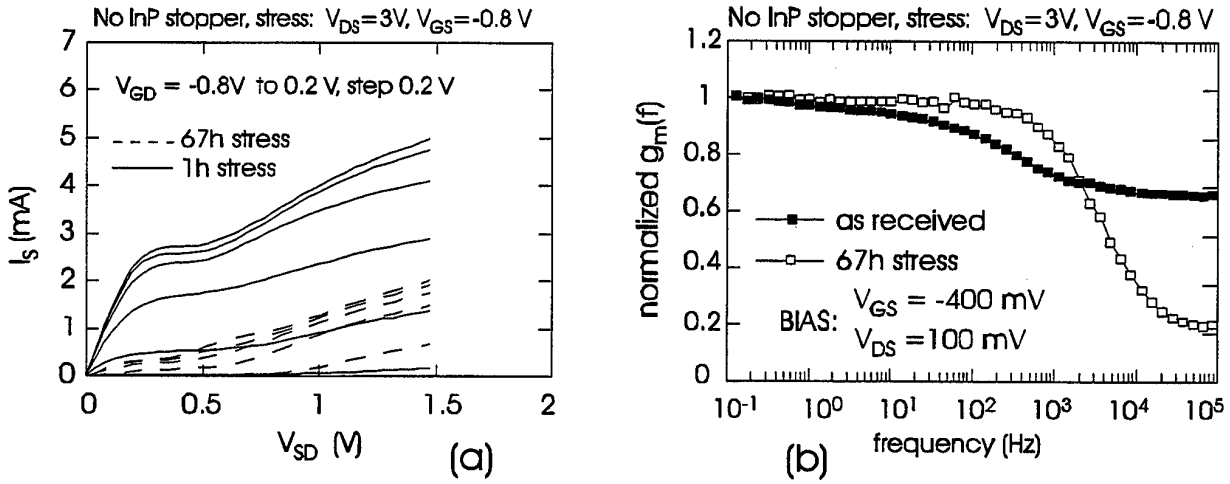

Figure 3.12: **(a)** I_S vs V_{SD} at different V_{GD}measured after 1 hr and after 67 hrs of stress at V_{DS} = 3 V, V_{GS} = -0.8 V, in a device without the InP etch-stopper. **(b)** g_m(f) measured before and after 67 hrs of stress at V_{DS} = 3 V, V_{GS} = -0.8 V in a device with the InP stopper.

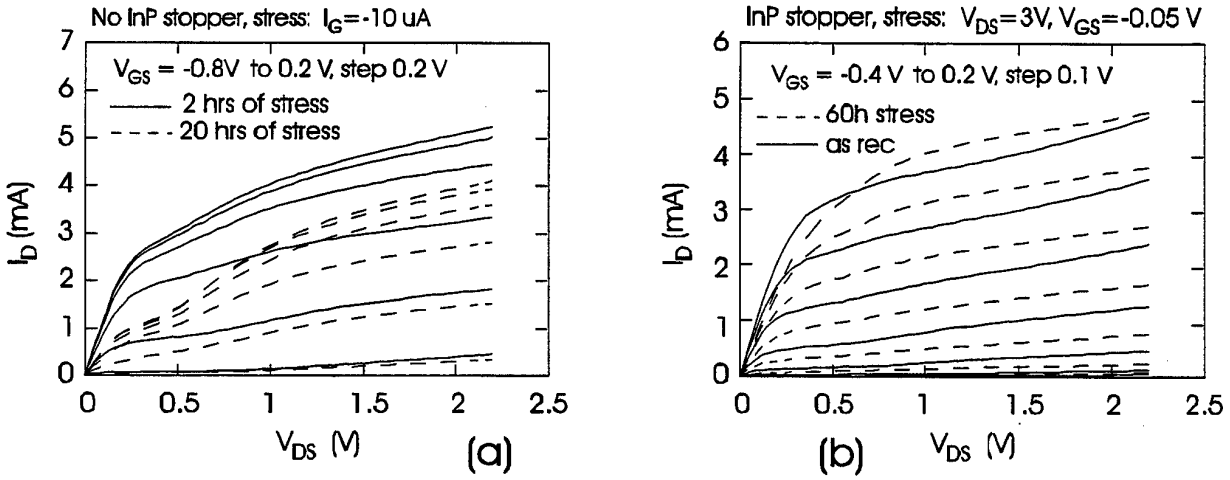

Figure 3.13: **(a)** I_D vs Vds at different V_{GS} measured after 2 hrs and after 20 hrs of stress at I_G = -10 mA (V_{DS} about 6 V), in a device without the InP etch-stopper. **(b)** I_D vs V_{DS} at different V_{GS} measured before and after 60 hrs of stress at V_{DS} = 3 V, V_{GS} = -0.05 V in a device with the InP etch-stopper.

hydrogen effects. After the initial phase, I_D stabilizes, and we did not observe either drain current degradation or g_m(f) dispersion up to 100 hours of test at V_{DS} = 3 V.

In conclusion, the data presented here demonstrate that the InP stop etch layer is a viable solution to the problem of V_{th} reproducibility which also contributes to both suppress kink effects in InP-based HEMT's and improve the long-term stability of these devices avoiding surface trap generation during the hot-electron stress test. We further confirm that kink effect in these devices can not be ascribed only to the pile-up of holes in the gate-to-source access region but is due to the simultaneous presence of traps and holes generated by impact ionization.

Part III

Impact-ionization and trap-related effects in 6H SiC JFETs

Chapter 4

Silicon Carbide JFET

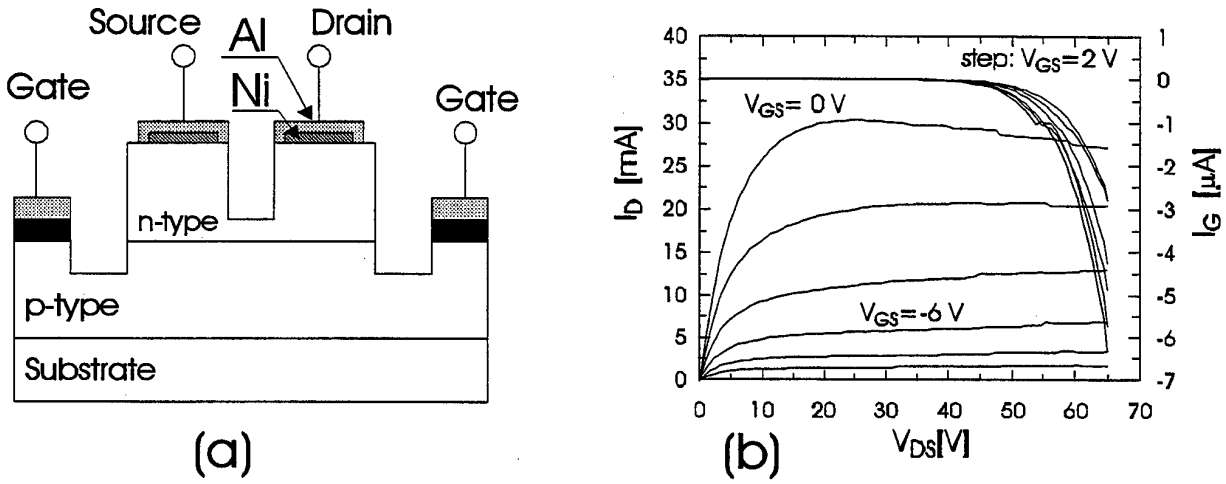

Figure 4.1: **(a)** Schematic cross section of the 6H-SiC JFET. **(b)** I_G, I_D vs V_{DS} at different V_{GS} . The decrease of I_D at high V_{DS} is due to device self-heating.

4.1 Introduction

The high-field behaviour of devices fabricated on wide band-gap semiconductors is closely related to parasitic effects induced by carrier capture and emission by deep levels or by partially ionized impurities, in the presence of impact-ionization. The aim of this work is to describe experimental results concerning on-state weak ionization effects, off-state gate-drain breakdown phenomena and low-temperature electrical anomalies in buried-gate 6H SiC JFETs. The study has been carried out using devices fabricated by vacuum sublimation epitaxy on high-quality 6H n-type SiC platelets grown by an unmodifed Lely process [136]. The Lely crystals are free of micropipes and have usually a much lower density of dislocations than wafers grown by other techniques, thus reducing the effects of these defects on device electrical characteristics [136].

We will show that: (i) impact-ionization in on-state conditions decreases with temperature, with a temperature coefficient of the multiplication factor $\simeq -7.5 \cdot 10^{-6} K^{-1}$; (ii) the observed decrease of the off-state gate-drain breakdown voltage at increasing the temperature can not therefore be attributed to an increase of ionization at higher temperatures, but derives from the presence of deep levels or partially ionized impurities [137]; (iii) another evidence of the presence of deep levels is represented by a kink in the output drain I-V characteristics, which appears at low temperatures (< -50°C) for high drain voltages, V_{DS} > 40 V. The kink is due to the compensation of negative charge trapped on surface traps or deep levels consequent to electric-field-induced detrapping or to injection of holes

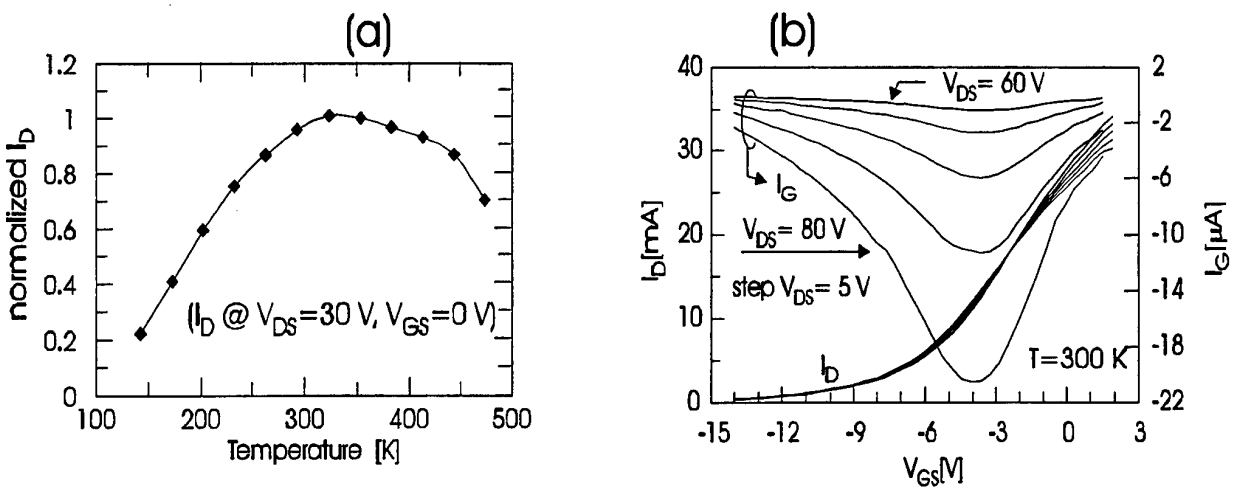

Figure 4.2: **(a)** I_D vs Temperature (normalized to the RT value) at V_{DS} = 30 V, V_{GS} = 0 V. **(b)** I_G, I_D vs V_{GS} at different V_{DS}. The bell shape behaviour demonstrates the presence of impact ionization.

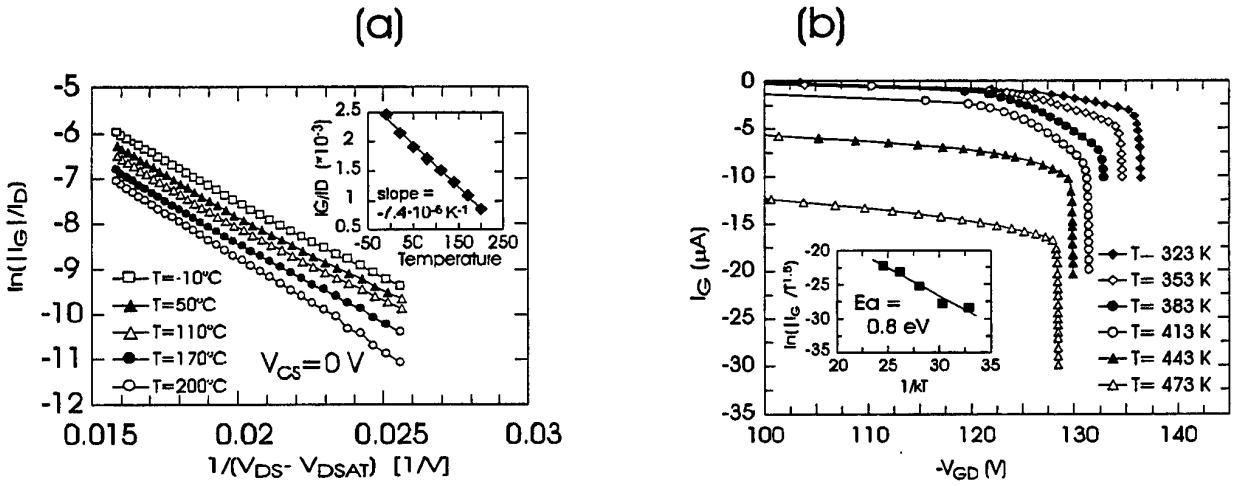

Figure 4.3: **(a)** ln(| I_G | /I_D) vs 1/(V_{DS} - V_{DSAT}) at different temperatures. In the insert: | I_G | /I_D at V_{DS} = 75 V as a function of temperature. **(b)** Gate-drain breakdown voltage (source floating) measured at different temperatures. Insert: Arrhenius plot of the reverse current before breakdown, at V_{GD} = -10 V, giving an activation energy Ea = 0.8 eV.

generated by impact-ionization; (iv) the kink is correlated with both a down-ward and an upward dispersion of the transconductance as a function of frequency, $g_m(f)$. Downward dispersion has Ea = 0.26 eV, which corresponds to a positive peak in the drain current DLTS spectrum, and can be attributed to process-induced deep levels on the surface of the source-drain recessed-channel region [138]. Upward dispersion has Ea = 0.20 eV and corresponds therefore to the ionization energy of Al acceptors in the p-doped gate layer, observed in current and capacitance DLTS spectra. Finally, (v), the current DLTS spectra show the presence of a peak at Ea = 0.15 eV, attributed to nitrogen donors in the n-channel layer [139].

4.2 Device description and analysis of DC Characteristics

Figure 4.1(a) shows a schematic cross-section of the buried-gate JFETs, with a p-gate doping density (Aluminum) $3 \cdot 10^{18}$ cm^{-3} and a n-channel doping density (Nitrogen) of $3 \cdot 10^{17}$ cm^{-3}, L=8 μm,

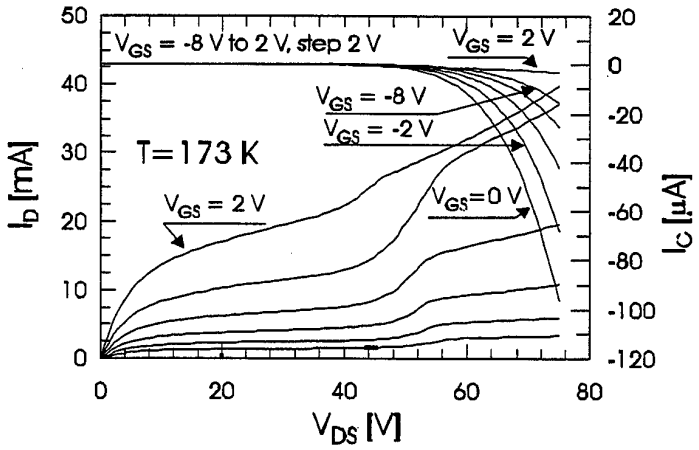

Figure 4.4: I_D, I_G vs V_{DS}measured at T=173 K showing the presence of a "kink" in I_D.

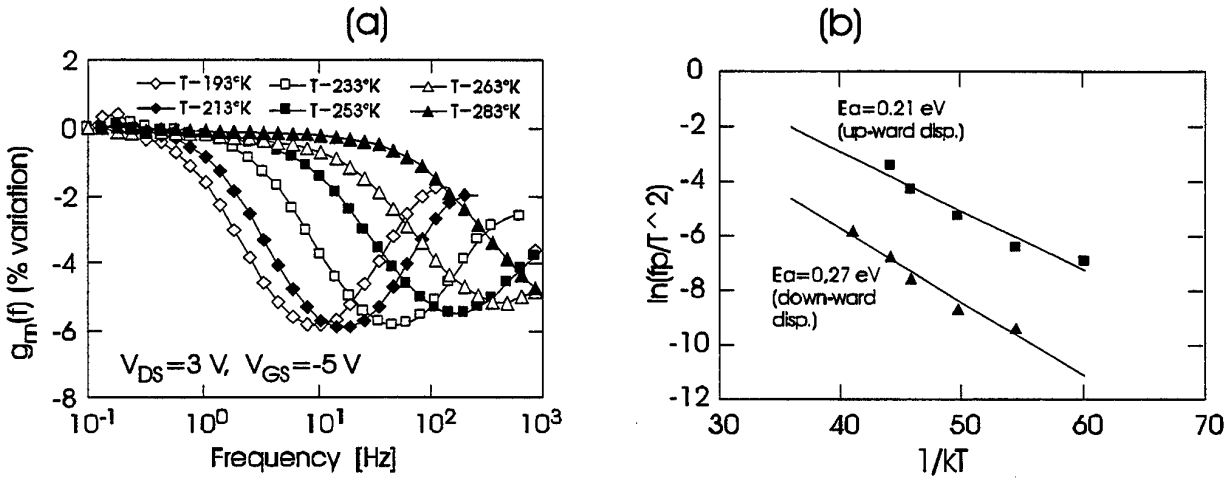

Figure 4.5: **(a)** $g_m(f)$ dispersion on buried gate 6H-SiC JFET. **(b)** Activation energy calculated from $g_m(f)$ dispersion measurements on buried gate 6H-SiC JFET.

W=0.76 mm. Fig. 4.1(b) shows the output characteristics of a representative sample, together with the gate current I_G, measured at Room Temperature, RT. At increasing V_{DS} beyond 40 V, a large increase in the (negative) I_G is observed, which is attributed to the collection of holes generated by impact-ionization, as occurs in GaAs FETs. To avoid device self-heating, which is evident in Fig. 4.1(b), pulsed measurement, with a duty cycle of 1% have been chosen in order to study devices characteristics as a function of temperature. The drain current I_D has a non-monotonic behaviour as a function of T, see Fig. 4.2(a), decreasing from RT towards low-temperatures due to the reduction in channel conductivity consequent to the decrease in donor ionization, and from RT towards higher temperatures due to the reduced electron mobility and drift velocity consequent to enhanced phonon scattering [140].

The on-state gate current vs V_{GS} shows the 'bell-shape' behaviour typical of impact-ionization, see Fig. 4.2(b). Carrier multiplication due to impact-ionization is usually modeled in FETs as $|I_G|/I_D \simeq \exp[-1/(V_{DS}- V_{DSAT})] \simeq \exp[1/(E \cdot L_{eff})]$, where L_{eff} is the effective length where ionization occurs, V_{DSAT} is the drain saturation voltage and E is the longitudinal electric field. The $|I_G|/I_D$ experimental data actually follow an exponential dependence on $1/(V_{DS} - V_{DSAT})$, as shown in Fig. 4.3(a). Since I_G is proportional to the hole current, while I_D represents the primary electron current, $|I_G|/I_D$ represents the impact-ionization multiplication factor, which decreases at increasing T, due

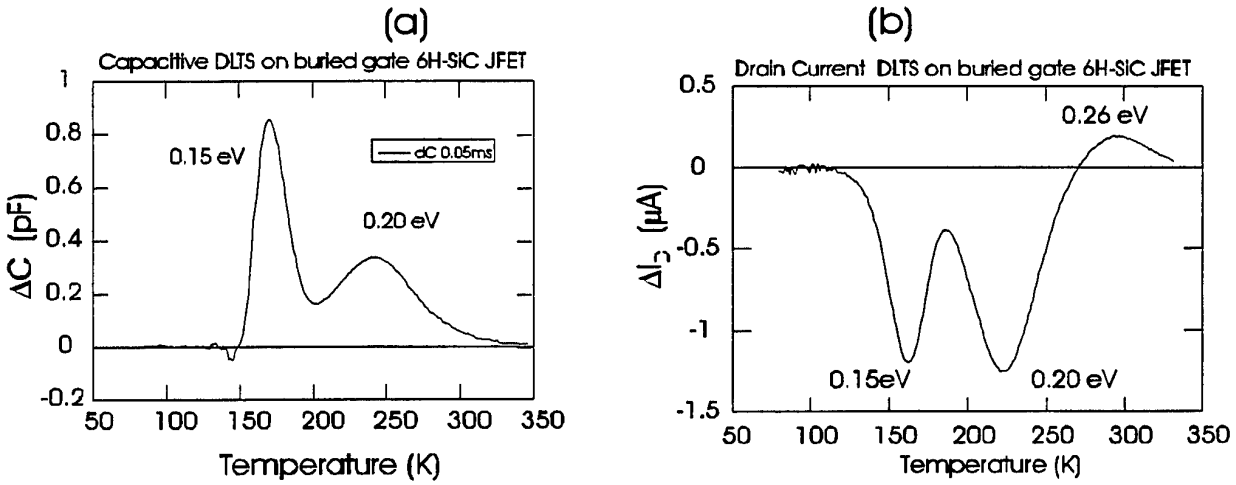

Figure 4.6: Capacitive DLTS (**a**), and Drain current DLTS (**b**), on buried gate 6H-SiC JFET.

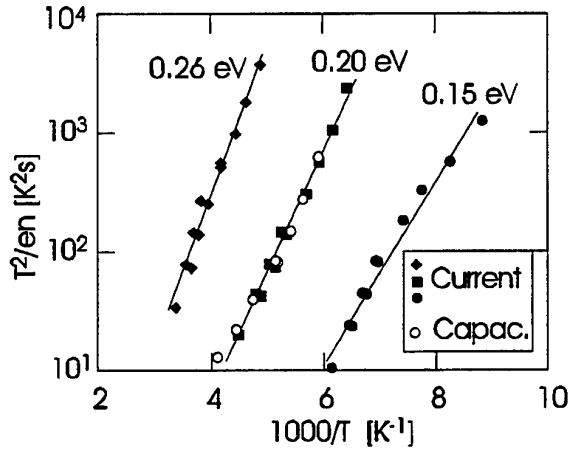

Figure 4.7: Activation energies evaluated from both drain current and capacitive DLTS on buried gate 6H-SiC JFET.

to increased phonon scattering and reduced electron energy.

The off-state gate-drain breakdown voltage, BV_{DG}, is close to the theoretical value [141], but decreases at increasing T, see Fig. 4.3(b). Since impact-ionization alone would have caused a positive coefficient of BV_{GD} as in the case of Si and GaAs devices, other mechanisms are present. In particular electron detrapping from surface states has been already reported to induce an increase in the electric field [142], while presence of incompletely ionized impurities has been shown to cause current lock-on [143]; both effects may eventually lead to device breakdown.

The presence of deep levels or of dispersion effects related to non-ionized impurities is also derived from the observation of kinks in the I_D - V_{DS} characteristics at $T < -50°C$, see Fig. 4.4. Kink occurs at $V_{DS} > 40$ V, when impact-ionization is triggered and can be attributed to the compensation of negative charge trapped on surface traps or deep levels consequent to electric-field-induced detrapping or to injection of holes generated by impact-ionization.

4.3 Traps in SiC JFET

Kink phenomena are correlated with both a down-ward and a upward dispersion of the transconductance as a function of frequency, $g_m(f)$, Fig. 4.5(a). Downward dispersion has Ea = 0.26 eV, Fig. 4.5(b), which corresponds to a positive peak in the drain current DLTS spectrum, Fig. 4.6(a), and is attributed to process-induced deep levels on the surface of the source-drain recessed-channel region [139]. Since these are surface traps, they do not contribute to the current DLTS spectrum of the gate/channel pn junction, compare Figs. 4.6(a) and 4.6(b). Upward dispersion of $g_m(f)$ has Ea = 0.20 eV and corresponds to the ionization energy of Al acceptors in the p gate layer, observed in both the drain current and capacitance DLTS spectra. The current DLTS spectra also shows the presence of a peak at Ea = 0.15 eV, attributed to nitrogen donors in the n-channel layer, see Figs. 4.6(b) and 4.7 [139]. The analysis reported here show for the first time a close correlation between DLTS results and device electrical characteristics of SiC JFETs and clearly demonstrate the influence of surface states and deep donors/acceptors levels in determining high field and low temperature behaviour and parasitic effects of SiC devices.

Part IV

Conclusions

Conclusions

The work carried out under the seed project"Study of Hot-Electron Effects, Breakdown and Reliability in FETs, HEMTs and HBTs" has provided new data, obtained by means of experimental work and Monte Carlo simulations, concerning the maximum voltage limitations of advanced microwave devices. In particular we have analyzed devices based on GaAs and InP (i.e. having the channel region composed by $In_{0.2}Ga_{0.8}As$ in pseudomorphic HEMT on GaAs, and by $In_{0.53}Ga_{0.47}As$ in lattice-matched HEMTs on InP, respectively) and JFETs grown on 6H SiC.

Some conclusive remarks can be listed here, summarizing the results of the work.

- InP-based HEMTs show the best performances for applications at 90 GHz and beyond, both in terms of noise and in terms of rf power and power added efficiency. Power applications for these devices are limited by factors related with device design and channel material properties;
- The narrow bandgap of $In_{0.53}Ga_{0.47}As$ induces significant impact-ionization even at low applied voltages, see Figs. 1.1 and 1.2 of this report;
- The electron impact-ionization coefficient, α_n, of $In_{0.53}Ga_{0.47}As$ does not follow the usual linear dependence on exp(1/F), where F is the electric field, so that ionization is non negligible even at low electric field, Fig. 1.2;
- The thermal coefficient of the impact-ionization is positive, see Fig. 1.3, (the thermal coefficient of breakdown voltage is negative), thus leading to potential electro-thermal positive feedback mechanisms which can induce premature breakdown and burn-out.

The poorness of the channel material properties concerning breakdown can be compensated by a clever design of the device structure (the following rules apply in particular to InP-based HFETs and HEMTs but can be used also to improve the breakdown voltage of devices based on GaAs or on wide bandgap materials):

- The off-state breakdown can be improved by increasing the barrier height of the gate Schottky junction, thus limiting thermionic emission of electrons from the gate to the channel, which starts the avalanche process in off-state conditions;
- Composite InGaAs/InP channel structures adopting channel quantization can be used to enhance the breakdown voltage of InP-based HEMTs, see Figs. 2.27 and 2.28;
- A suitable gate recess structure can reduce the longitudinal electric field, thus improving both on-state and off-state breakdown voltage;
- On-state breakdown voltage can be also improved if removal or control of holes generated by impact-ionization is obtained. In fact, holes induce a pseudo-bipolar effect which is responsible of kink effects and premature breakdown in on-state conditions, see Figs. 2.14 and 2.17.

Very high values of the on-state and off-state breakdown voltages can be obtained, of course, by adopting wide bandgap semiconductors, such as SiC. The technology of these devices, as well as that

of GaN microwave devices, is rapidly improving. Initially, the measured breakdown voltages were much lower than the ideal ones, mostly because of the presence of premature breakdown points due to a high density of micropipes. With the improvement of epitaxial techniques this problem has been partially reduced. Several authors, however, have shown anomalous breakdown voltages, with values which were decreasing at increasing temperature. Our work has been limited so far to buried gate JFETs grown on Lely substrates. Results show that:

- the multiplication factor $| I_G | / I_D$ and, consequently, the electron impact-ionization coefficient decrease at increasing temperature (the usual behaviour observed in both Si and GaAs)
- Several anomalous effects have been observed, such as: frequency dispersion of the transconductance and kink effects at low temperature. Moreover, the off state breakdown voltage decreases at increasing the temperature. These effects seems to be linked to the presence of incompletely ionized impurities and, possibly, of deep levels, as suggested by DLTS measurements, see Fig. 4.6.

Reliability problems can also limit the applicability of all kind of FET devices at high voltages, due to failure mechanisms induced by hot carriers. During this work we have carried out extensive device accelerated testing and we identified failure mechanisms induced by hot carriers in both GaAs-based pseudomorphic HEMTs and InP-based HEMTs. In particular:

- Trap creation in the gate recess region of pseudomorphic HEMT has been observed after hot carrier testing, giving rise to kinks in the output I-V characteristics, drain current and transconductance decrease, increase of transconductance frequency dispersion.
- Drain resistance increase and degradation of the access regions has been found in InAlAs/InGaAs HEMTs on InP. Surface degradation with trap creation seems to be responsible for the damage.

In general, a careful control of the characteristics of surfaces and interfaces seems to be crucial for a good hardness against hot carrier degradation, the most critical region being the recessed gate area, where surface damage may also be induced by plasma treatments. The adoption of an InP 'passivation' layer on top of the InAlAs greatly improves the reliability of InP HEMTs, see Fig. 3.13(b).

A better understanding of the physical phenomena which induce device breakdown and degradation effects is required if improved devices are to be fabricated. In the course of this project we demonstrated the capabilities of advanced experimental tools (such as energy-resolved and spatially-resolved electroluminescence measurements) and theoretical simulation programs (a 2D Monte Carlo device simulator) in describing hot carrier transport in advanced microwave devices. Further work is needed

- to understand in more detail the physics of on-state breakdown effects
- to understand dynamic effects and degradation under pulsed conditions
- to derive models which allow one to predict reliability in operating conditions from DC and rf accelerated tests data to analyze possible reliability problems due to deep levels in wide bandgap devices.

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